

Microfabrication glass and Si

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μFLOW CELL
Scaling Microfluidics to
Industrial Applications

Which materials?

Assignment

- Which material would you recommend or exclude for the following applications?

1. Microreactor for the field of organic chemistry, and conducting reactions using **aggressive organic solvents**
2. Single use device to analyze biomolecules from blood samples, and **detect** them **using optical means**
3. Microfluidic platform for the **electrical characterization** of particles using **integrated electrodes**

Which materials?

1. **Microreactor** for the field of organic chemistry, and conducting reactions using **aggressive organic solvents**

Answer: Aggressive solvents ⇒ **glass**

Chemical glassware based on glass since this material is the most resistant to aggressive solutions

2. **Single use** device to analyze biomolecules from **blood** samples, and detect them using **optical** means

Answer:

Optical detection ⇒ transparent material (glass, transparent polymer)

Single use device, blood samples ⇒ **transparent polymer**

3. Microfluidic platform for the **electrical** characterization of particles using **integrated** electrodes

Answer:

Electrical detection ⇒ insulating material (no silicon)

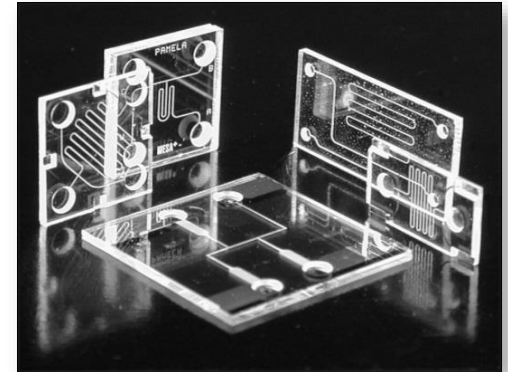
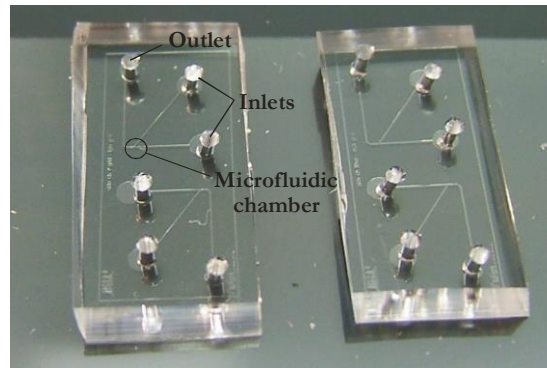
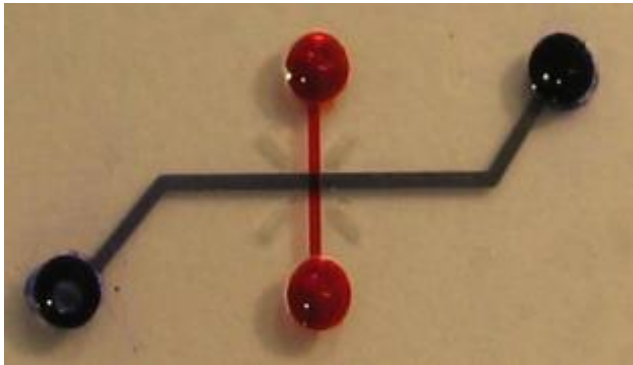
Integrated electrodes ⇒ cleanroom fabrication ⇒ **glass**

Important material properties ?

- **Material availability:** fabrication processes available for silicon and glass; flat wafers commercially available
- **Transparent materials:** optical techniques mostly used for the detection; possible observation of the samples.
- **Good insulators** (electrical/heat): frequent use of electric and thermal fields
- **Low permeability:** else, sample evaporation (the smaller, the worse) and changes in concentrations
- **Low background fluorescence:** else, interference with detection schemes (fluorescence most sensitive technique)
- **Low cost materials:** use of disposable devices (cheaper than device recycling)

Basic structure flow device

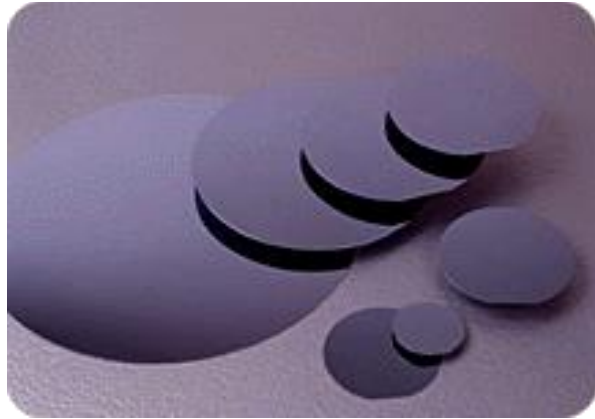
- 2 substrates $\Rightarrow$ closed environment
- 1 substrate including the channels/microfluidic structures
- 1 substrate = lid of the device
- Fluidic access $\Rightarrow$ reservoirs



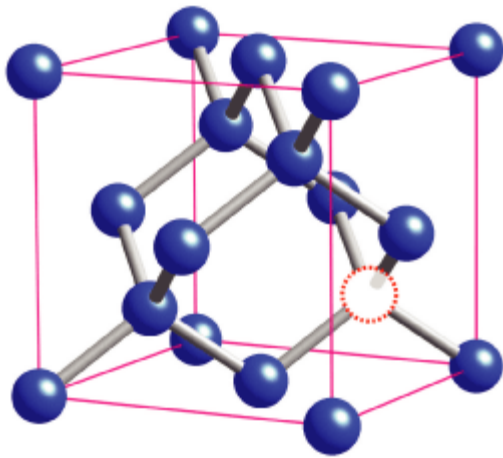
Fabrication steps:

- Realization of channels and microfluidic structures
- Machining of the fluidic accesses
- Bonding of the two substrates

Silicon

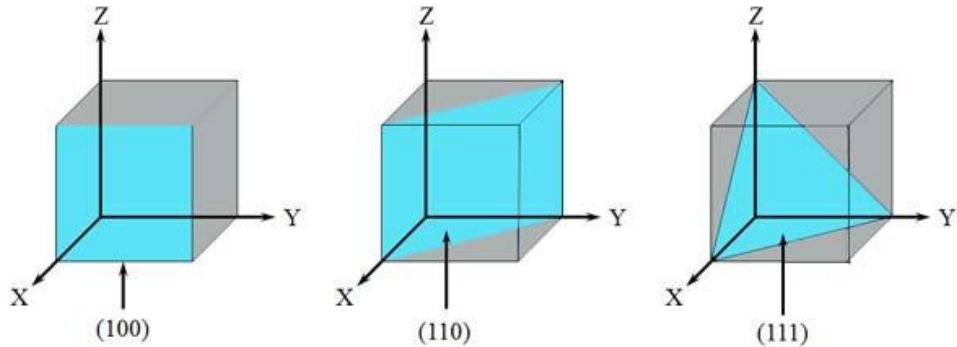


www.xbitlabs.com



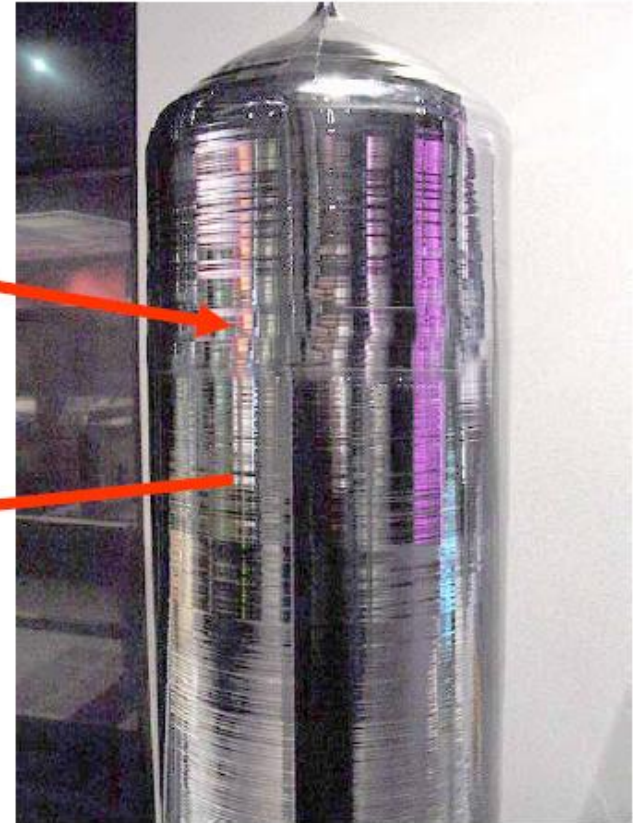
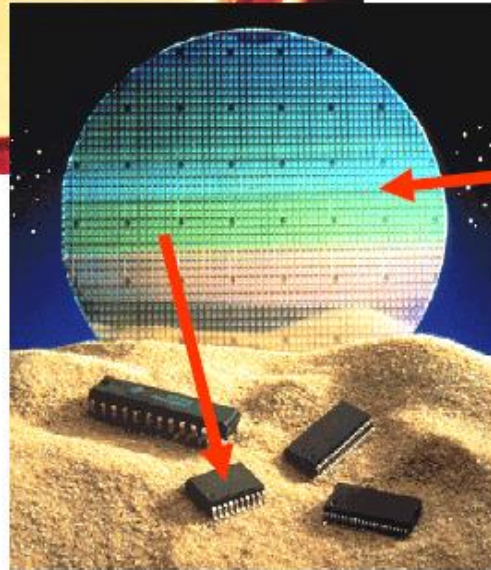
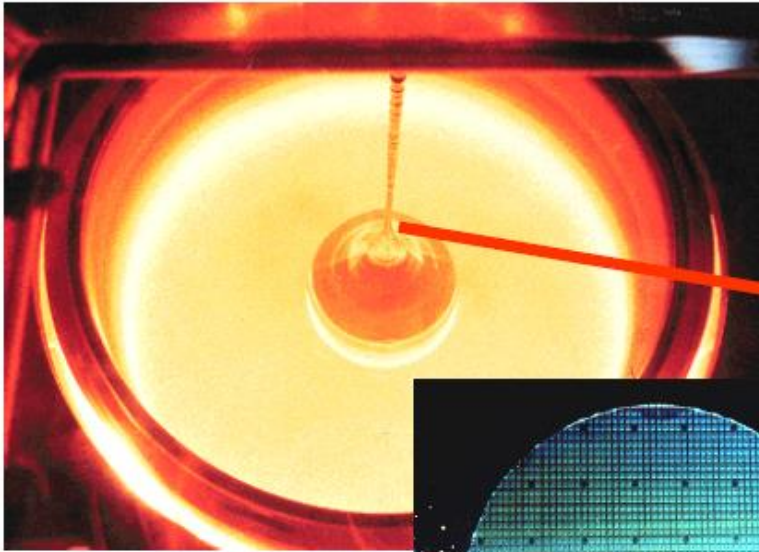
<http://jpsj.ipap.jp>

- Crystalline material processed as wafers
- Semi-conductor material: “holes” in the crystalline structures
- Different crystalline structures for silicon (100); (110) or (111)
 - ⇒ Impact on structures produced by wet-etching and on surface chemistry



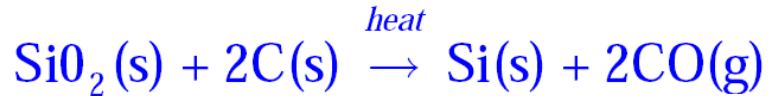
- Silicon mostly doped (n- or p-doped with e.g., B, As, P)
 - ⇒ Modification of its conductivity properties

From molten Si to IC chips



Electronic grade Si

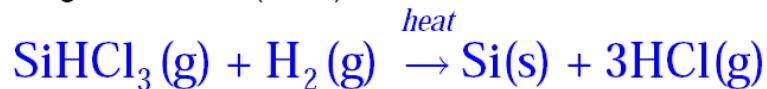
1. Quartzite is placed in a furnace with carbon releasing materials, and reacts as shown, forming metallurgic grade silicon (MGS):



2. MGS is then treated with hydrogen chloride to form trichlorosilane:

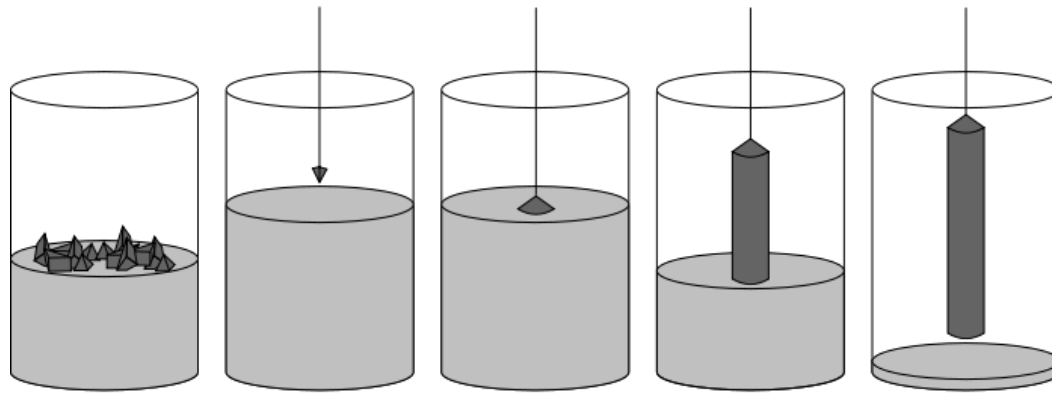


3. Next fractional distillation reduction with hydrogen produces electronic grade silicon (EGS):

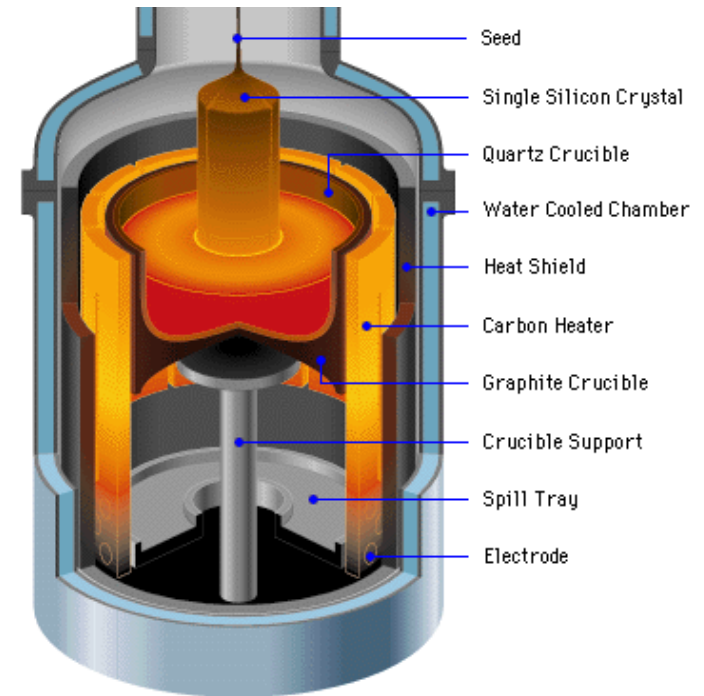


High-purity, semiconductor-grade silicon (only a few parts per million of impurities) is melted down in a crucible, which is usually made of quartz. Dopant impurity atoms such as boron or phosphorus can be added to the molten intrinsic silicon in precise amounts in order to dope the silicon, thus changing it into n-type or p-type extrinsic silicon. This influences the electrical conductivity of the silicon.

Czochralski method (CZ)



Seed pulled at 2-5 cm/hr



A **seed crystal**, mounted on a rod, is **dipped into the molten silicon**. The seed crystal's rod is pulled upwards and rotated at the same time. By precisely controlling the temperature gradients, **rate of pulling and speed of rotation**, it is possible to extract a large, single-crystal, cylindrical ingot from the melt.

This process is normally **performed in an inert atmosphere, such as argon, and in an inert chamber, such as quartz.**

Finally: dicing and grinding into wafers (2.5 cm tot 40 cm diameter)

$T > 1900\text{ }^{\circ}\text{C}$

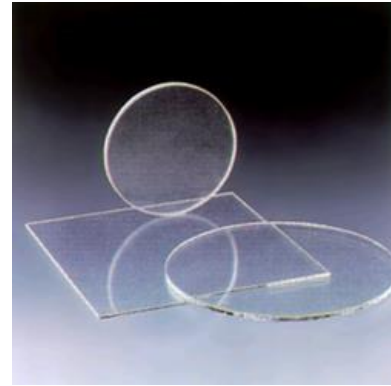
Glass

Quartz made from pure SiO_2

- High thermal resistivity and transparent to UV radiation
- Used as photolithography mask plates, thin film substrate, and other special applications
- Anisotropic etching problematic

Borosilicate glass

- Corning 7740™, Borofloat™, Tempax™...
- Thermal expansion coefficient matched to silicon
- Borosilicate wafers used for bonding with silicon wafers
- Very low background fluorescence



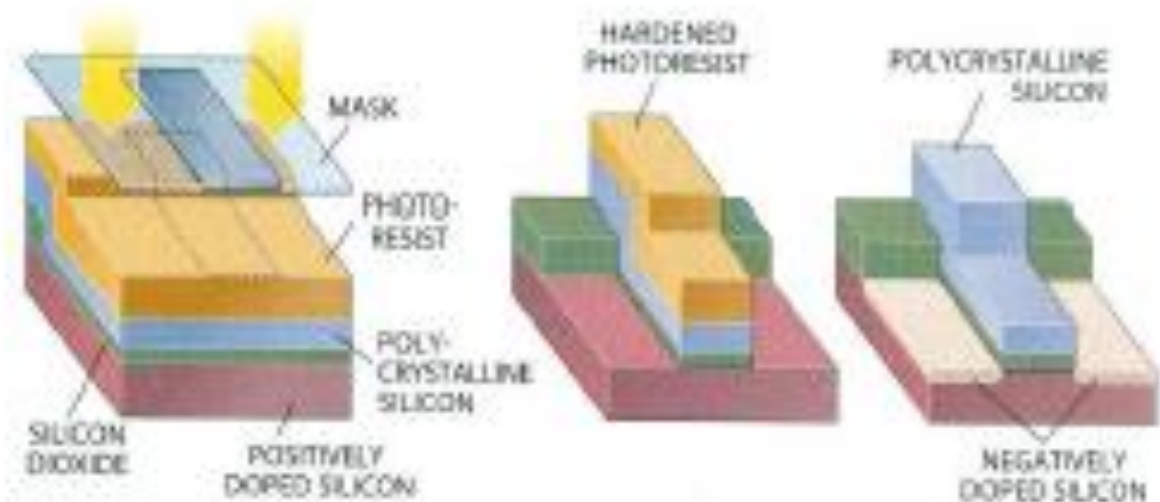
Li-Al silicate glass (Foturan™)

- Amenable for photostructuring due to special composition
- Fine structures down to 5-10 μm with high aspect ratios (1:30)
- Not TEC matched to silicon

IC technology

- cleaning
- deposition
- apply photoresist
- exposure
- development
- etching
- remove resist

100's STEPS



Cigarette smoke

- ... contains **10.000.000** dust particles per cubic foot ($\approx 27\text{l}$)
- clean air only **100.000**
- operating room less than **1000**
- **Q:** how many dust particles per cubic foot in an IC foundry?
- **A:** Less than **1!**



Cleanroom

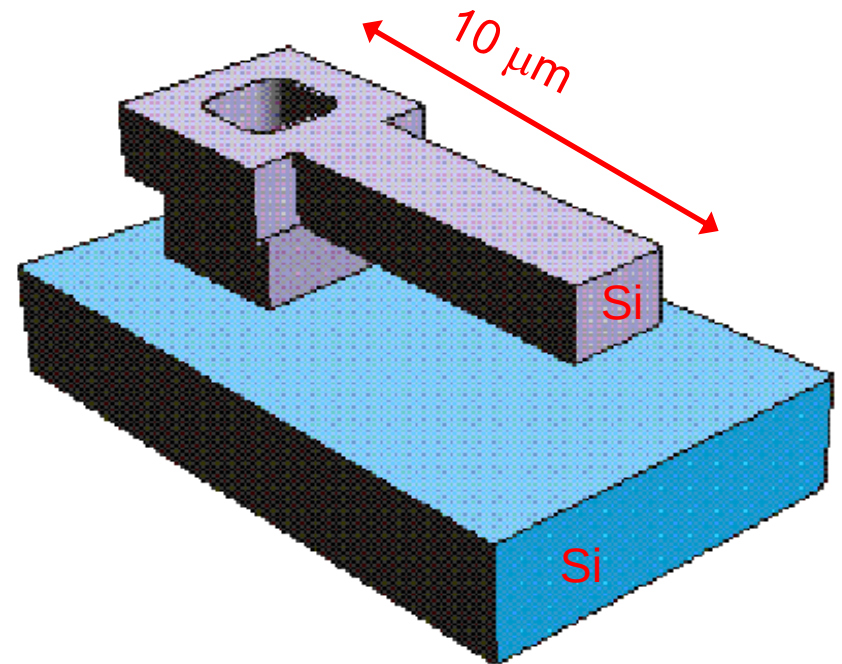
- **constant top-down flow of filtered air**
- **all air is replaced several times a minute**
- **wear gore-tex 'bunny suits' all the time**



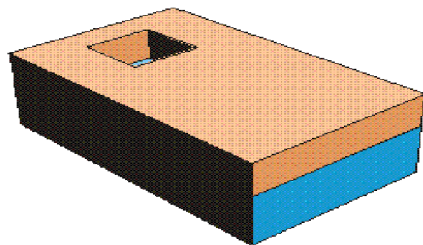
MEMS fab overview

How do you make this?

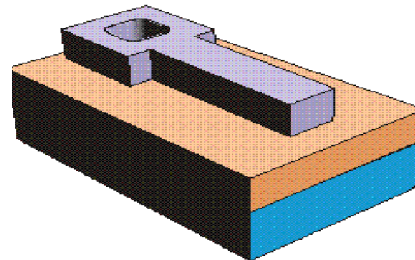
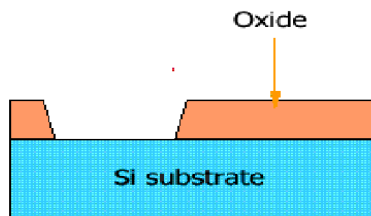
- using only 2D layer addition and removal
- with available processes
- micron-level size



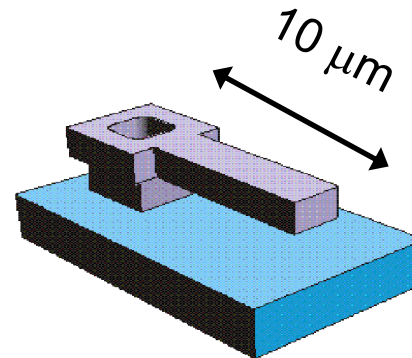
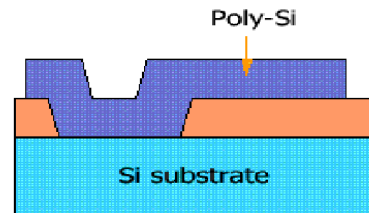
MEMS fab overview



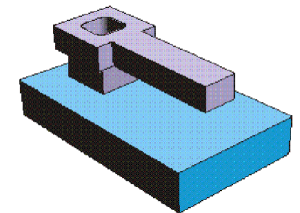
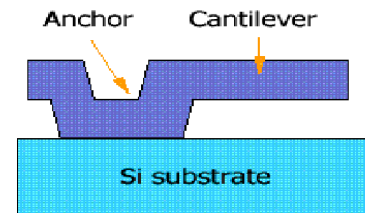
*Grow or
Deposit & pattern oxide*



Deposit & pattern poly



Sacrificial etch



W. Tang - Darpa

Overview processes

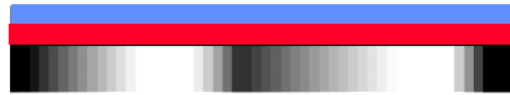
- Lithography
- Etching
- Deposition
- Bonding
- Increasing surface area

LITHOGRAPHY

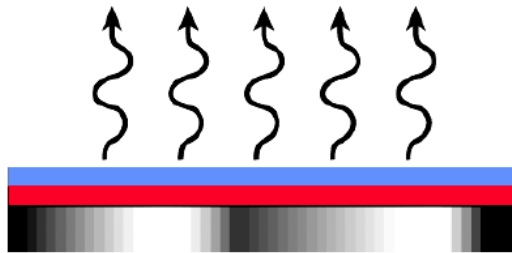
Photolithography



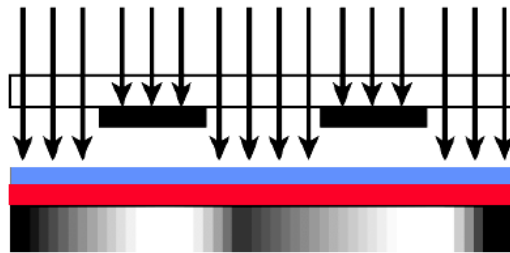
(1) Starting wafer with layer to be patterned



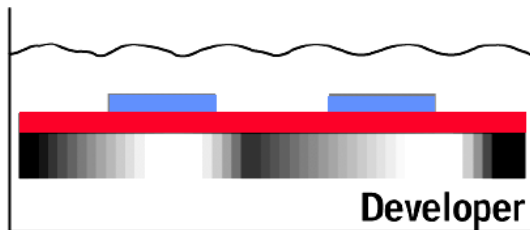
(2) Coat with photoresist



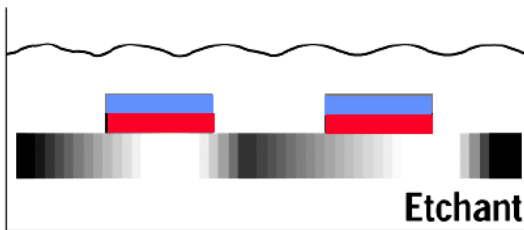
(3) Bake the resist to set its dissolution properties



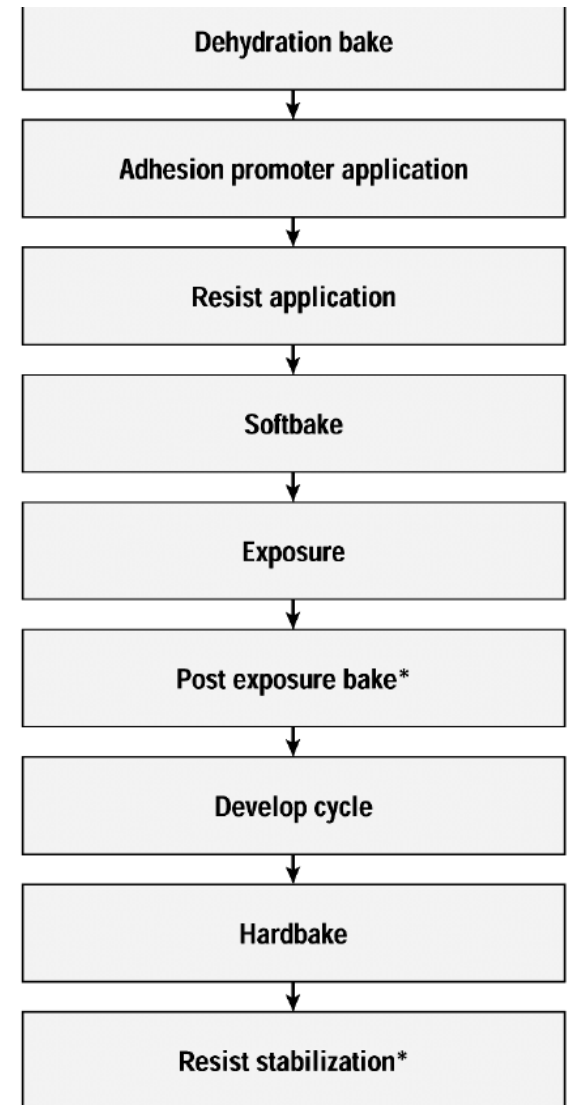
(4) Expose resist by shining light through a photomask



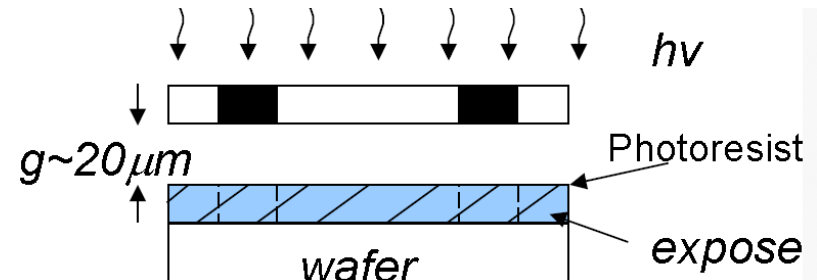
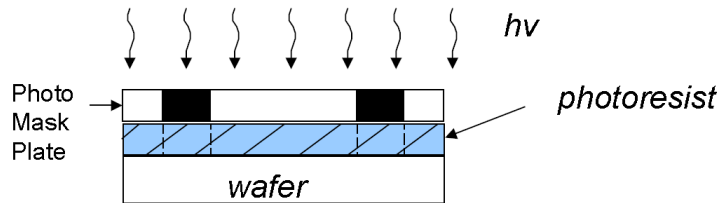
(5) Immerse exposed wafer in developer



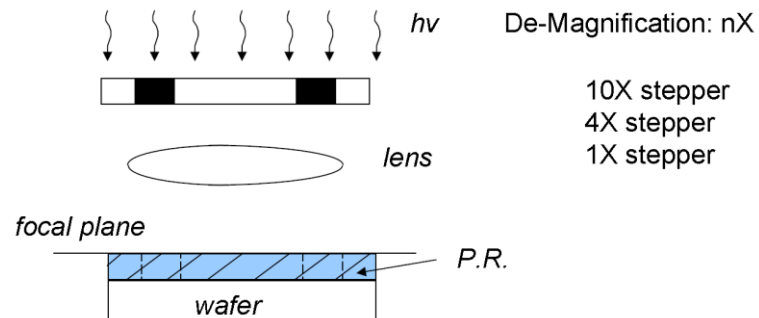
(6) Etch the film



Contact-proximity-projection

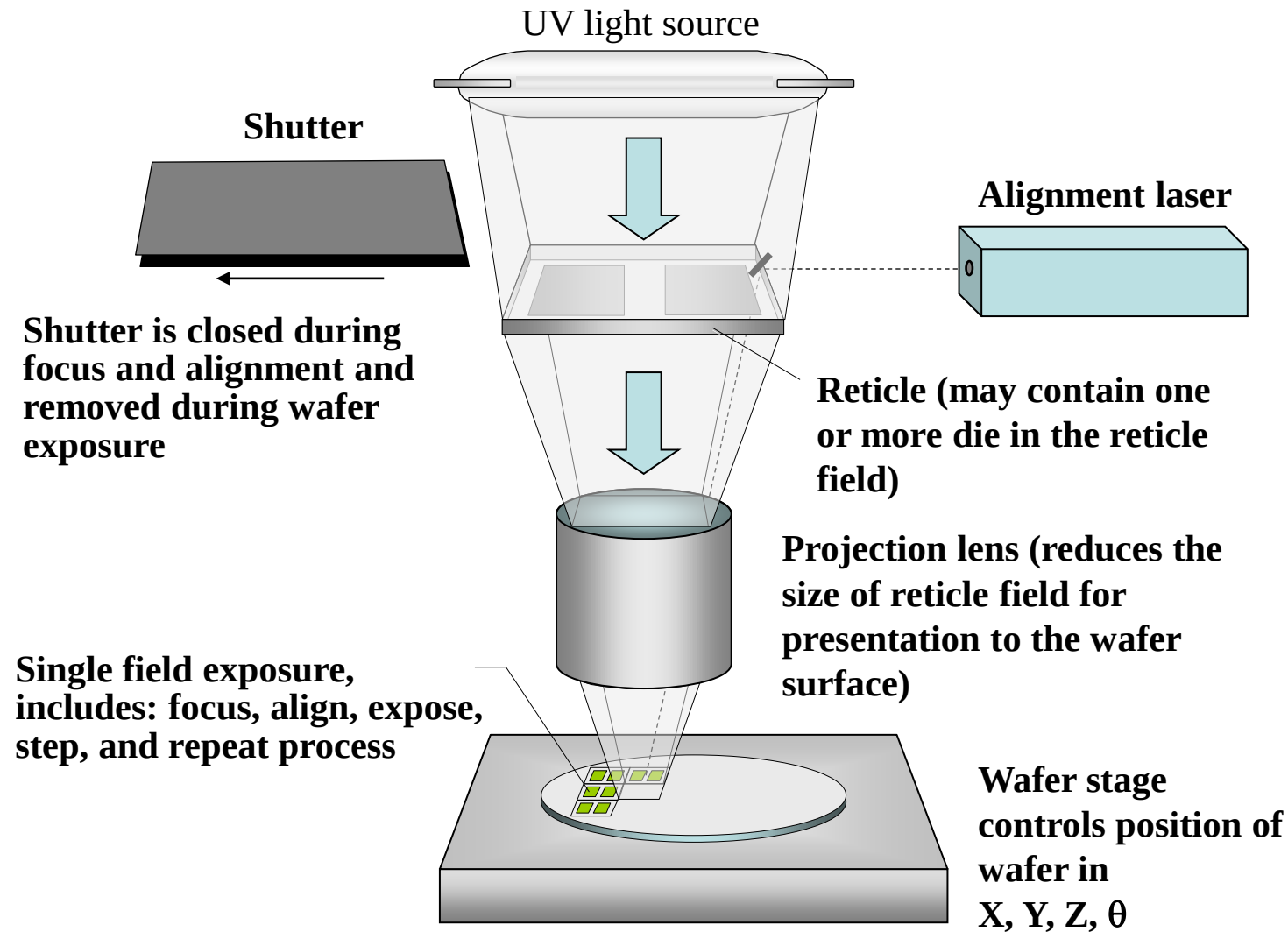


- Resolution $R < 0.5\mu\text{m}$
- mask plate is easily damaged or accumulates defects



$\sim 0.2\mu\text{m}$ resolution (deep UV photons)
tradeoff: optics complicated and expensive

Reticle pattern transfer to resist



Deep UV equipment

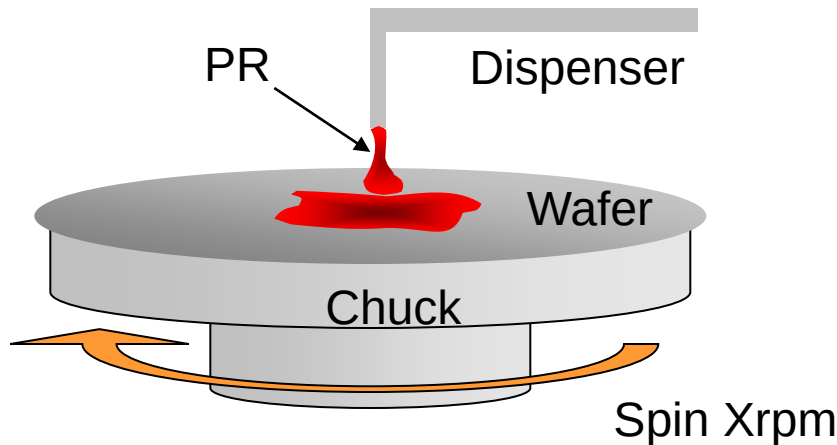
Example: ASML TWINSKAN™ XT:1250

- ASML: Veldhoven, Netherlands
- Sub wave length Lithography
- 193 nm KrF Laser (Deep UV)
- 65 nm resolution
- < 8 nm overlay
- > 85 WpH (300 mm)
- DOF ~ 0.50 μm (1: 600.000)
- price around 5M€
- www.asml.com

Assuming 'pixel size' of 65x65nm, writing a 300mm wafer is equivalent to 16×10^{12} pixels (16 Tera-pixels)

Photolithography

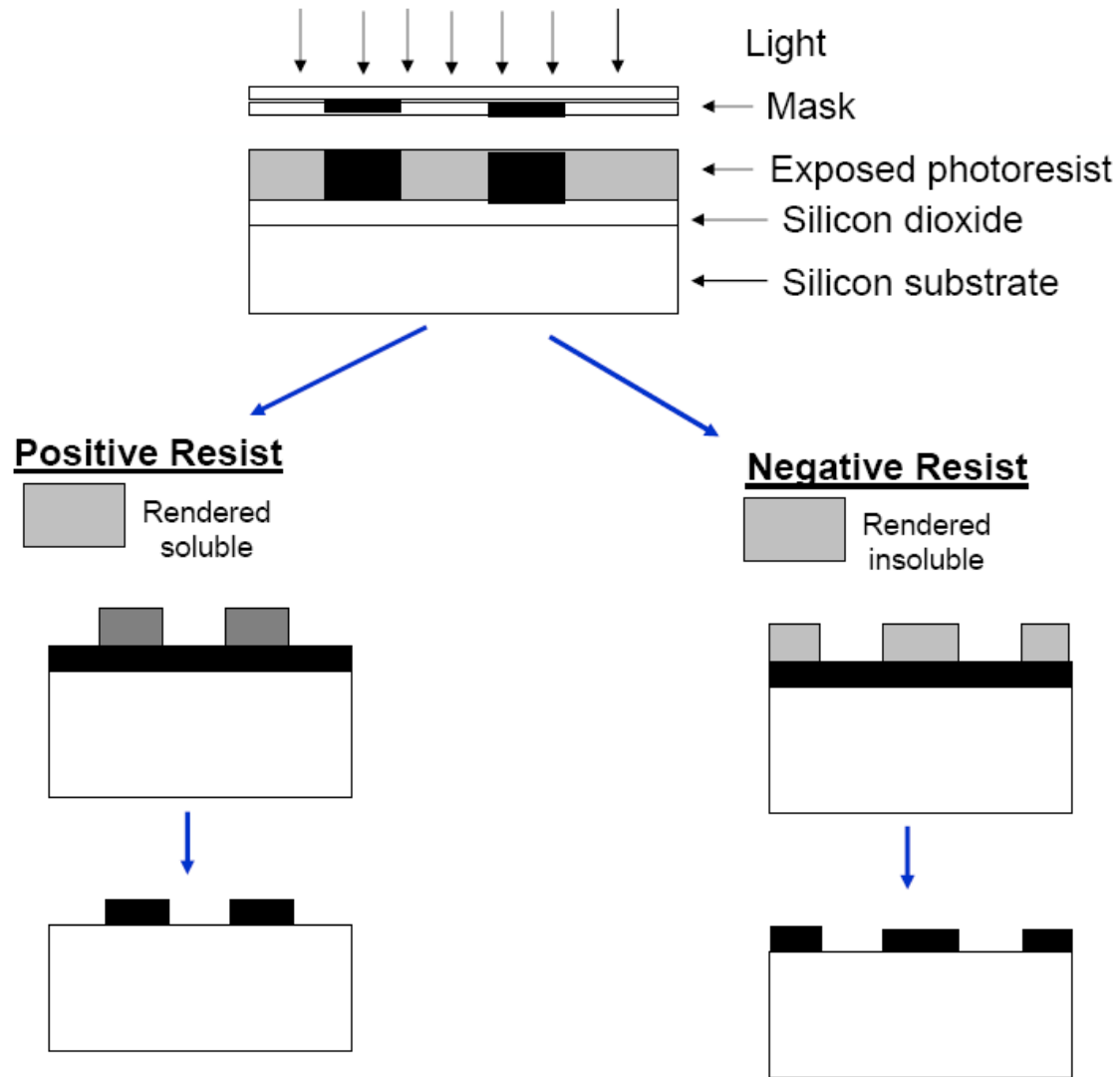
- “Photoresist” (PR) used to transfer patterns
- Viscous PR spun onto wafer
 - Dispense, then spin
 - Speed controls thickness
- Thickness: 0.5 – 30 μm
- Requires baking ($\sim 100^\circ\text{C}$)



7 μm Positive Thick Resist

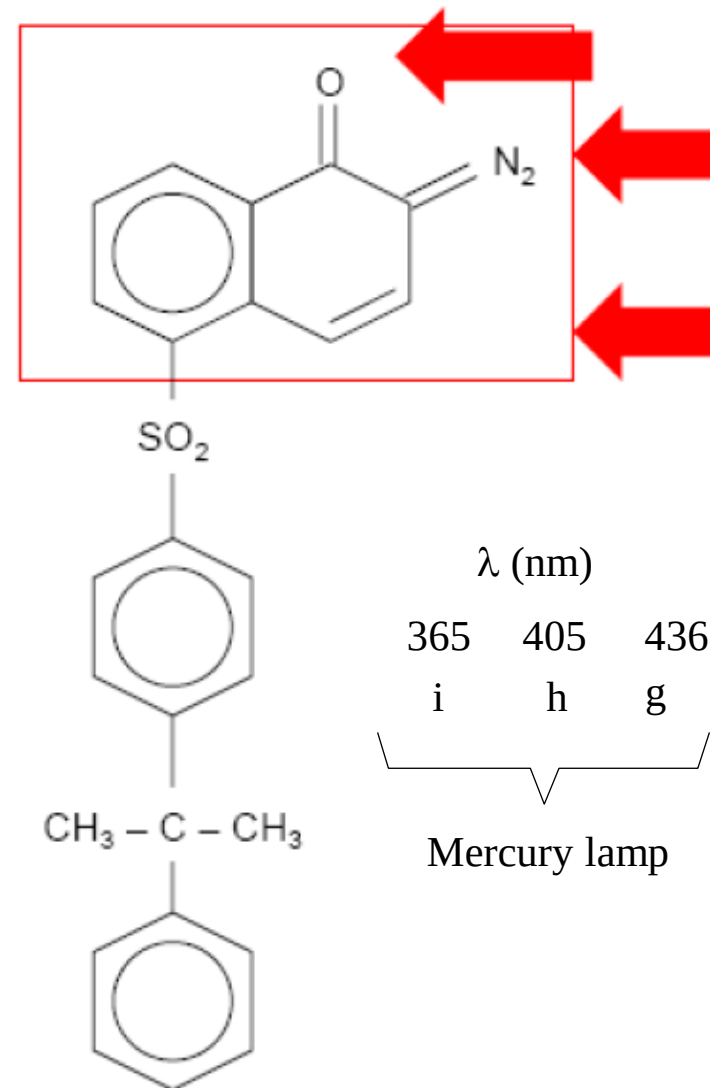
1. Dispense, Spin 3500rpm
2. Pre-bake 90°C 60min
3. UV mask expose 15 sec
4. Develop in aqueous solution
5. Post-bake 90°C 30min

Positive & negative resist



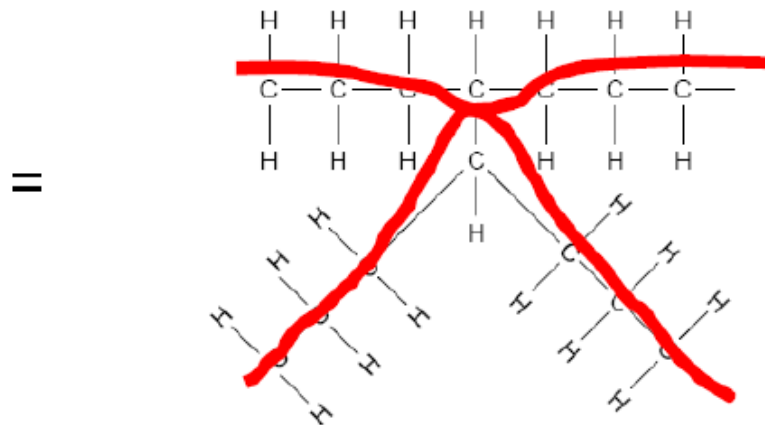
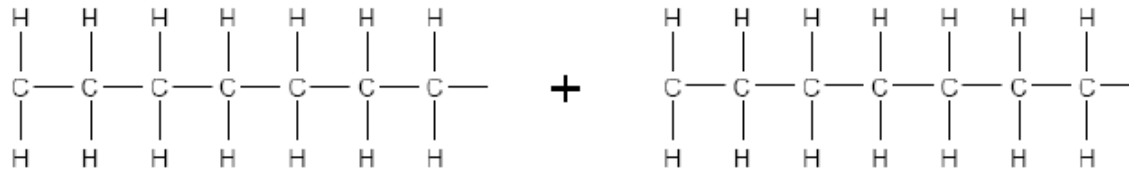
Lithography: positive resist

- Photochemical reaction during exposure weakens the polymer by rupture of the main and side polymer chains (e.g. loss of cross-linking).
- Exposed resist becomes more soluble in developing solutions; e.g. development rate for exposed resist is approximately 10 times the unexposed resist.
- Aqueous based developer: KOH, TMAH



Negative resist

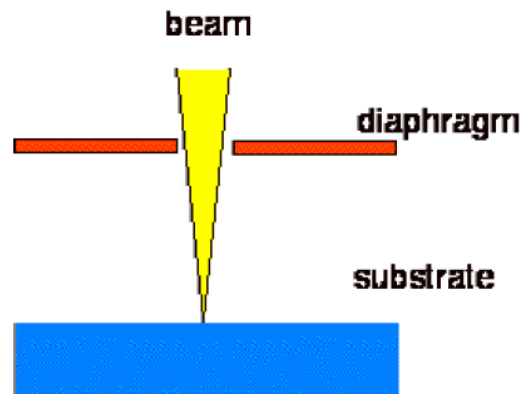
- Exposure of negative PR strength the polymer by random cross-linkage of main chains or pendant side-chains.
- Becomes less soluble (slower dissolving)
- Developer usually some solvent



E-beam lithography

resolution factors

- beam quality (~1 nm)
- secondary electrons (lateral range: few nm)

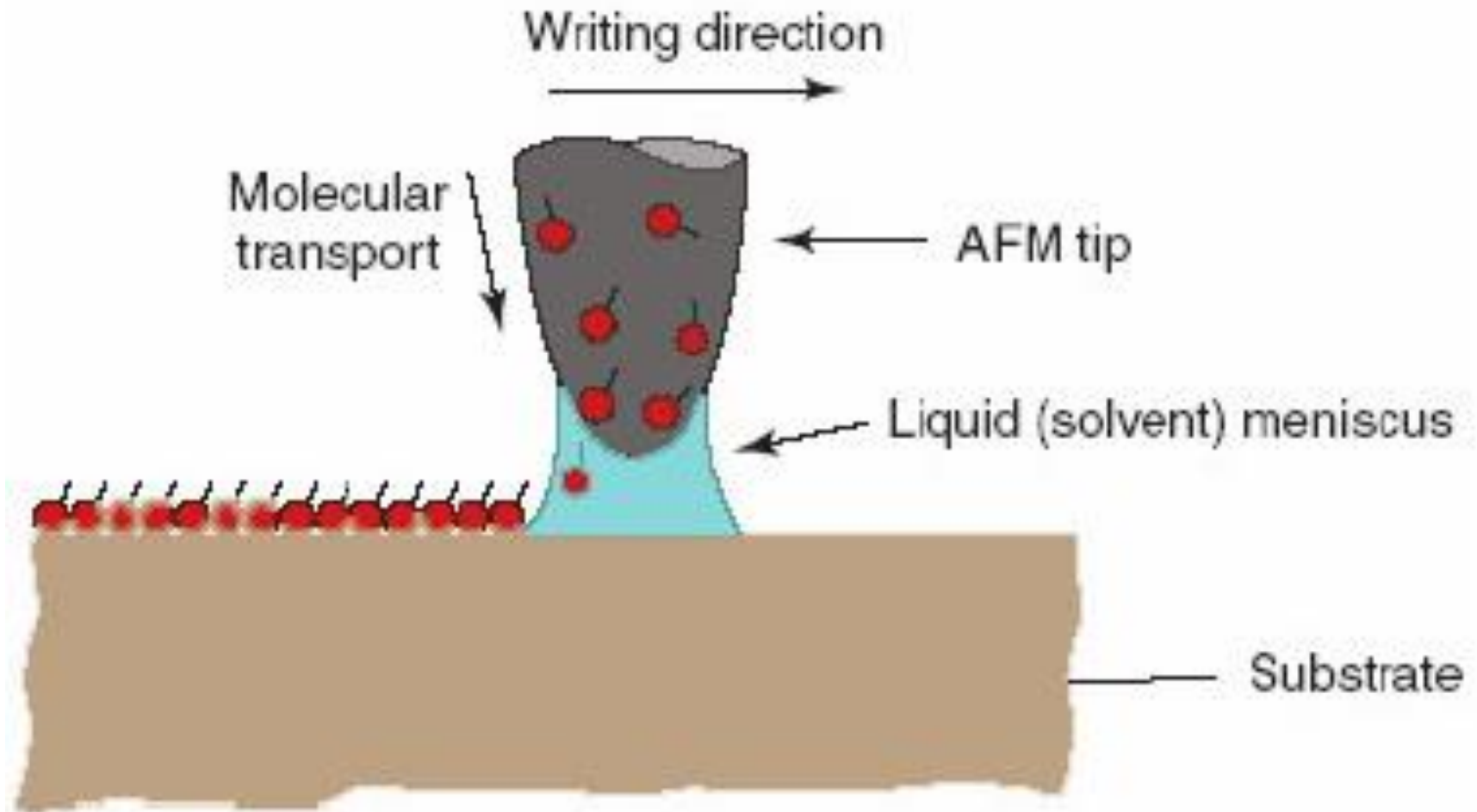


performance records

organic resist PMMA ~ 7 nm

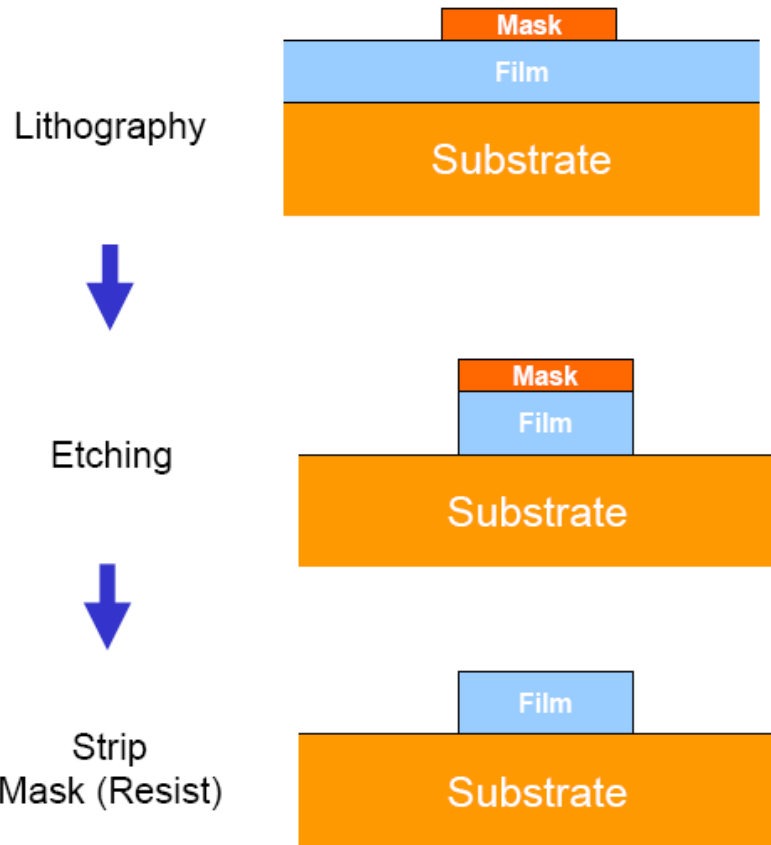
inorganic resist, b.v. AlF_3 ~ 1-2 nm

Dip-pen nanolithography

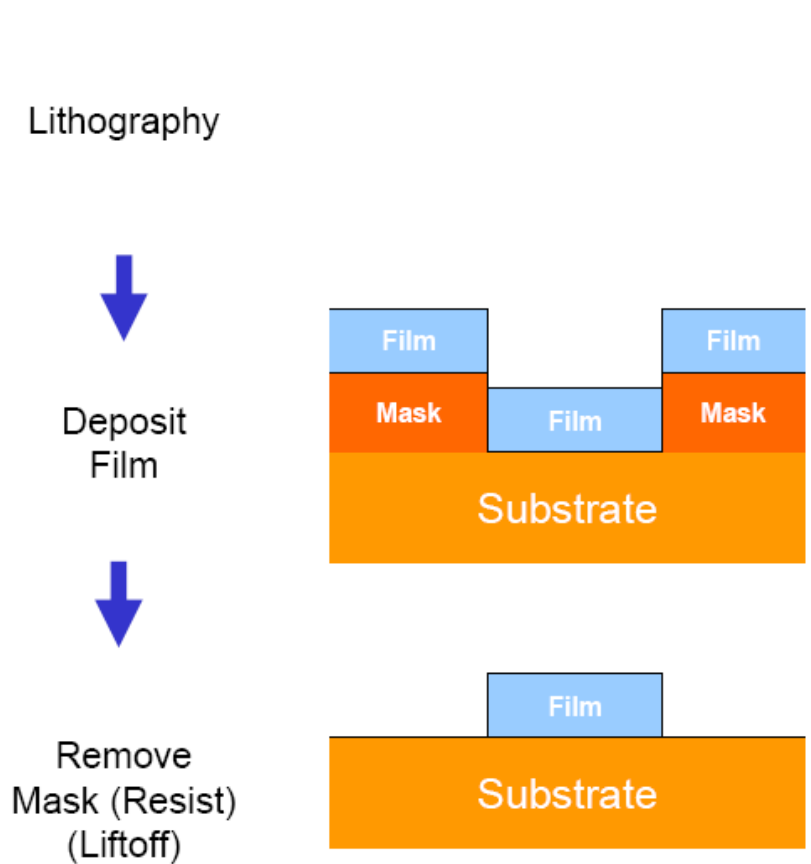


Etching vs. lift-off

Etching

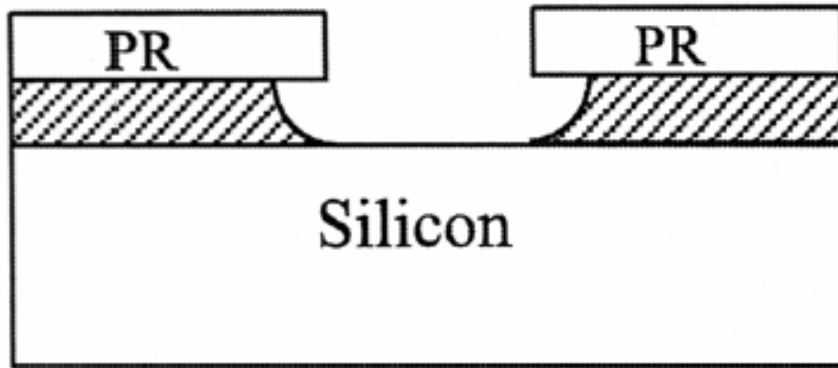


Liftoff



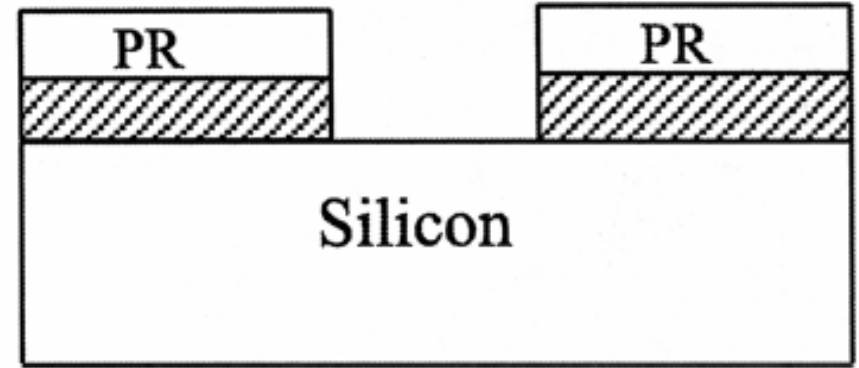
ETCHING

Etching profiles



(a)

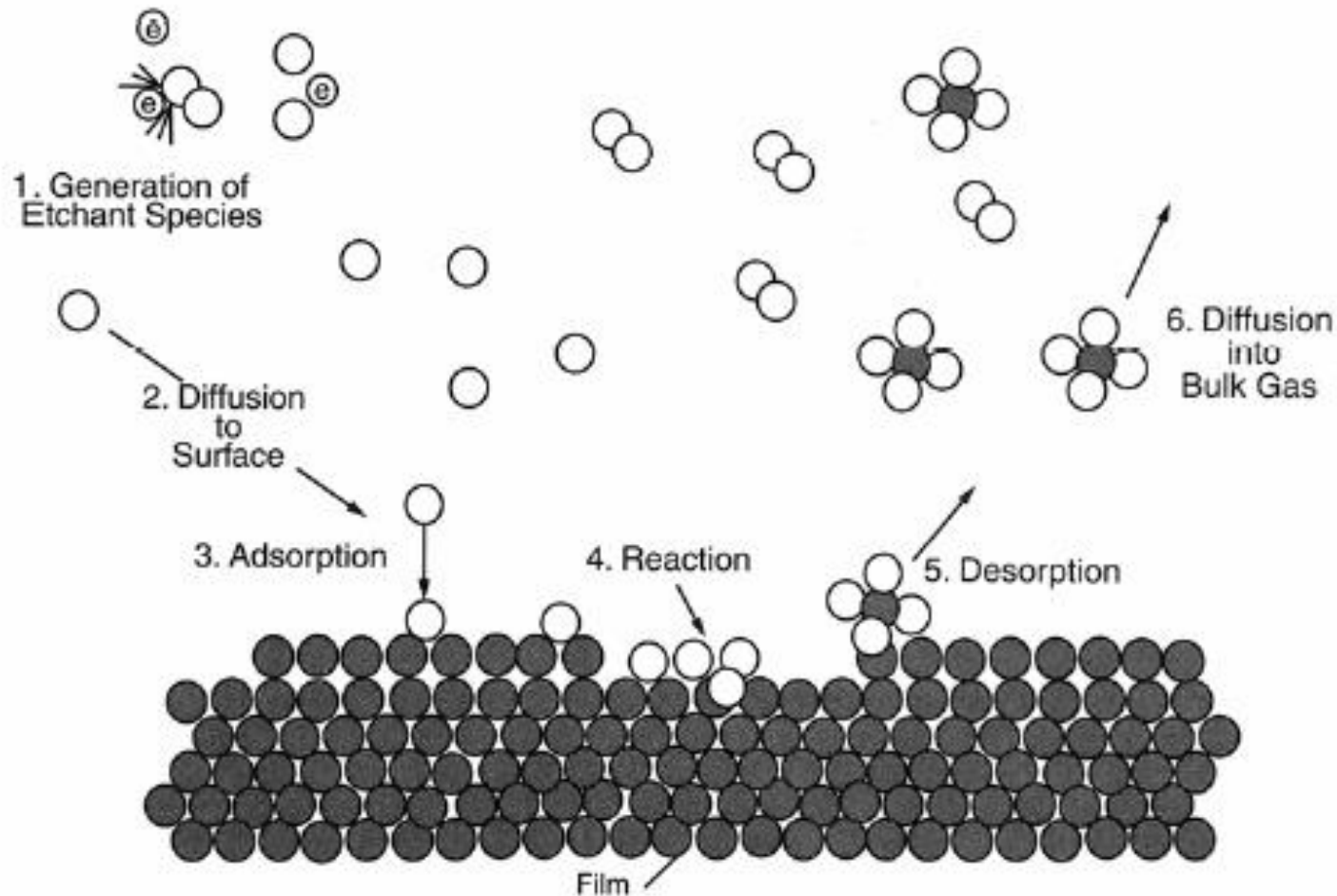
Isotropic Etching



(b)

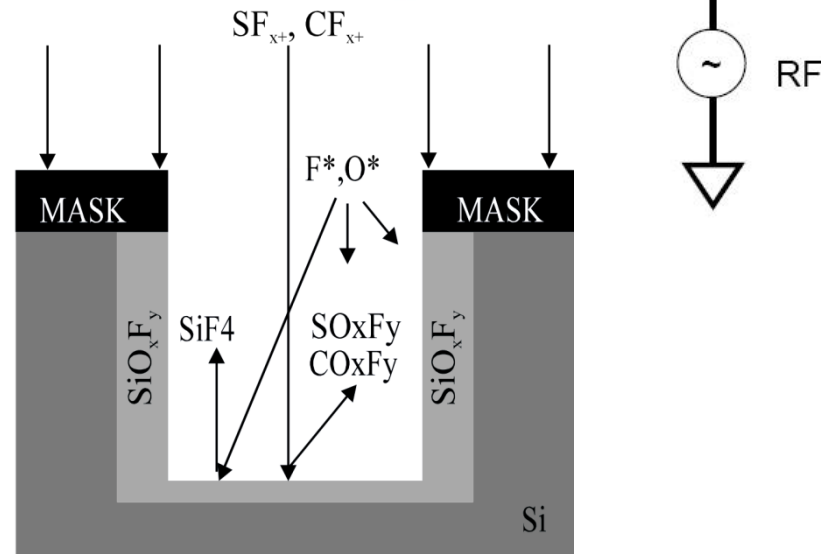
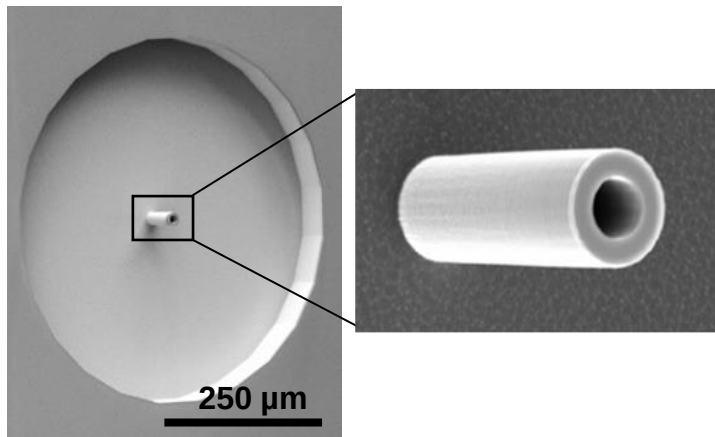
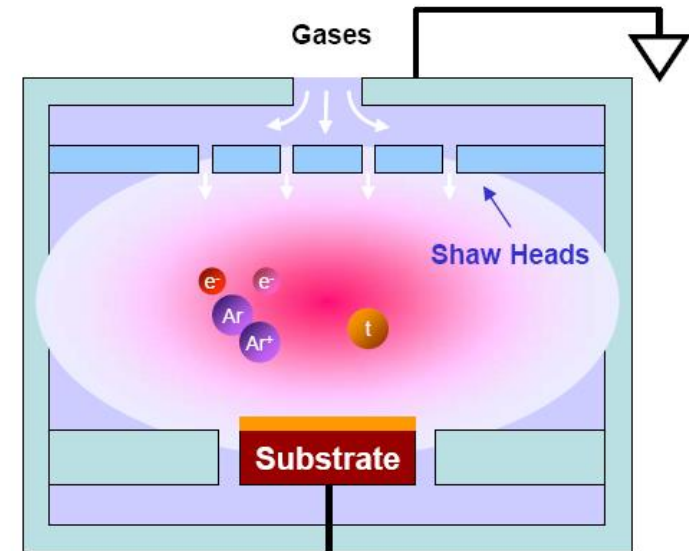
Anisotropic Etching

Dry etching (using a plasma)



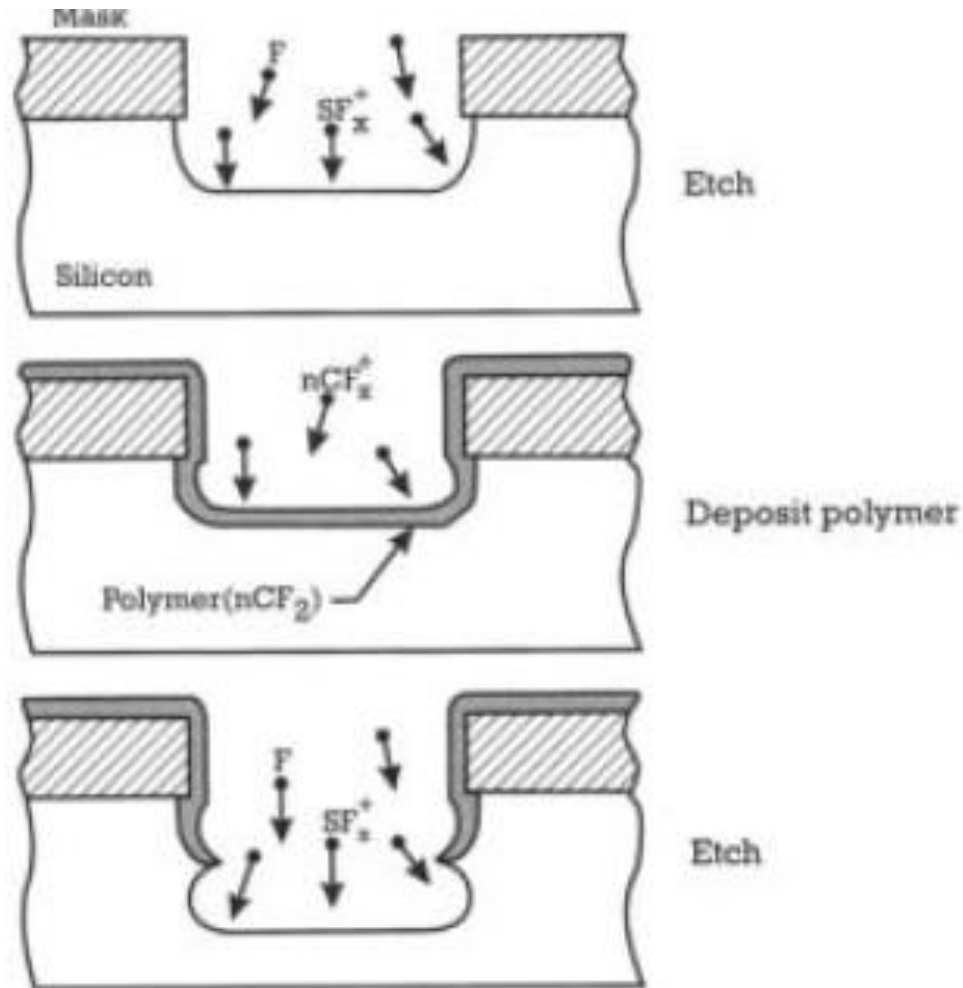
Deep reactive ion etching

- SF_6 gas etches the silicon
- Sidewall passivation (C_4F_8 polymer or O_2)
- Isotropic or anisotropic, depending on the machine settings!
- Etch rate $> 5 \mu\text{m}/\text{min}$



Courtesy Advion Biosciences

Bosch[®] process

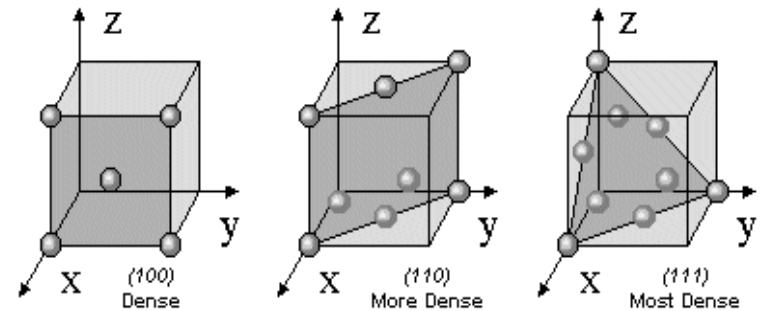


Anisotropic wet etching (Si)

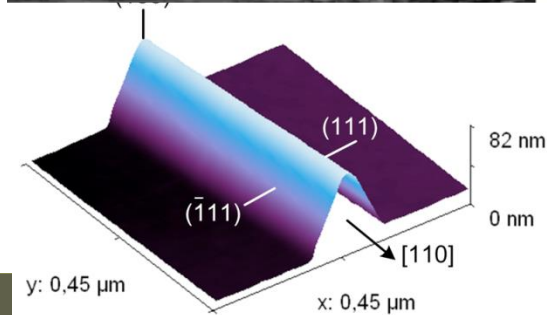
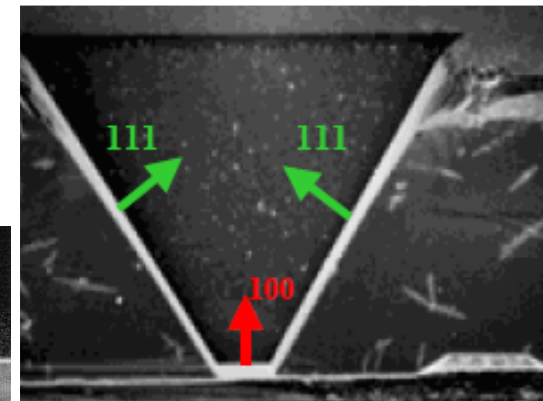
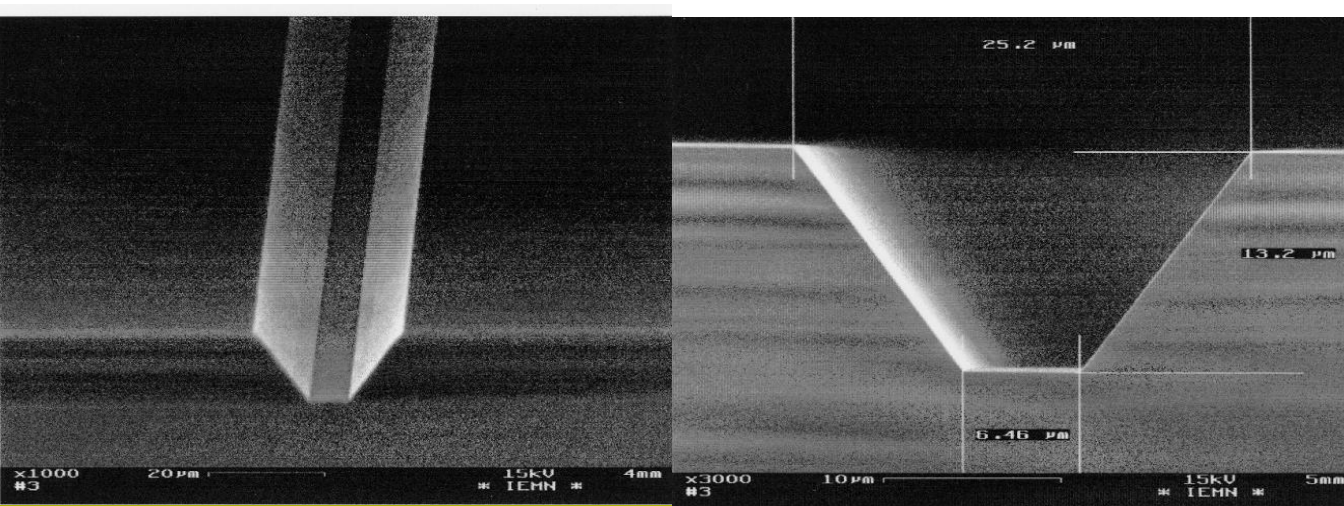
Etch mask: Si_3N_4 or SiO_2

- 25% KOH in water at 75° C
- $\langle 100 \rangle$ etches about $1\mu\text{m}/\text{min}$
- Selectivity over $\langle 111 \rangle$ plane is about 1:100

Miller indices identify crystal planes from the unit cell:



$\langle 100 \rangle$ wafers



Courtesy E. T. Carlen

Hydrofluoric acid (for SiO₂)

- Selective (room temperature)
 - etches SiO₂ and not Si
 - will also attack Al, Si₃N₄,...
- Rate depends strongly on concentration
 - maximum: 49% HF ("concentrated") ~ >2 μm/min
 - controlled: 5 to 50:1 ("timed") ~ <0.1 μm/min
- Dangerous !
 - not a strong acid
 - deceptive (looks just like water)
 - penetrate skin (adsorption) and attacks slowly
 - will target bones
- Etch Geometry
 - completely isotropic (used to undercut/release)
- Reactions:
$$\text{SiO}_2 + 6\text{HF} \rightarrow \text{H}_2\text{SiF}_6(\text{aq}) + 2\text{H}_2\text{O}$$

Selective laser etching

- Subtractive laser technology
 - Femtosecond laser irradiation: modifications in focal point of laser
 - Chemical etching

Laser-induced breakdown and damage in bulk transparent materials induced by tightly focused femtosecond laser pulses

Chris B Schaffer¹, André Brodeur¹ and Eric Mazur¹

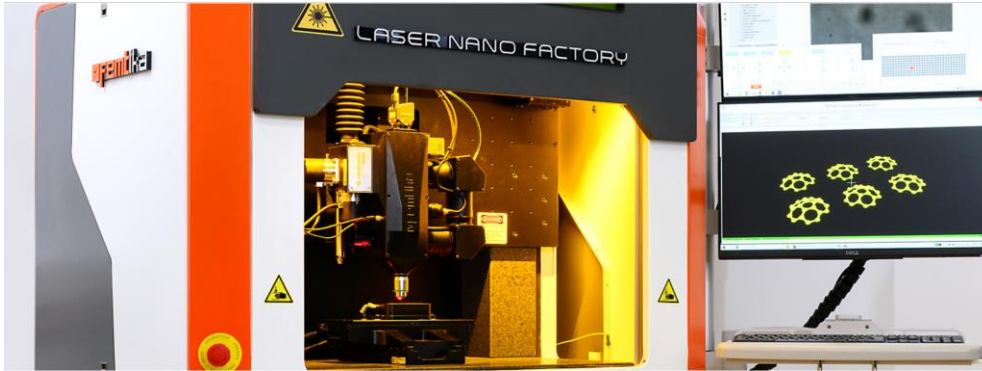
Published 9 October 2001 • Published under licence by IOP Publishing Ltd

[Measurement Science and Technology, Volume 12, Number 11](#)

Citation Chris B Schaffer *et al* 2001 *Meas. Sci. Technol.* **12** 1784

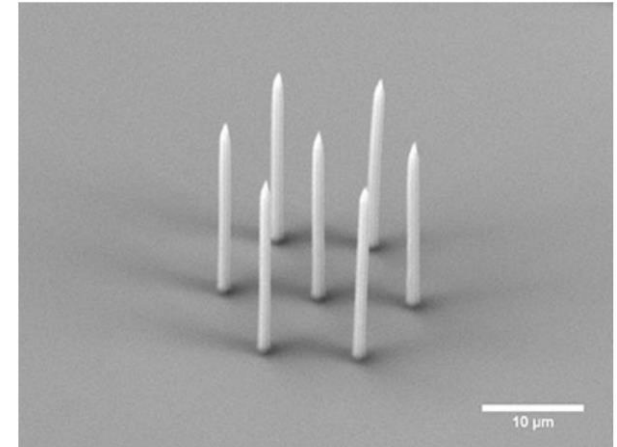
DOI 10.1088/0957-0233/12/11/305

Selective laser etching

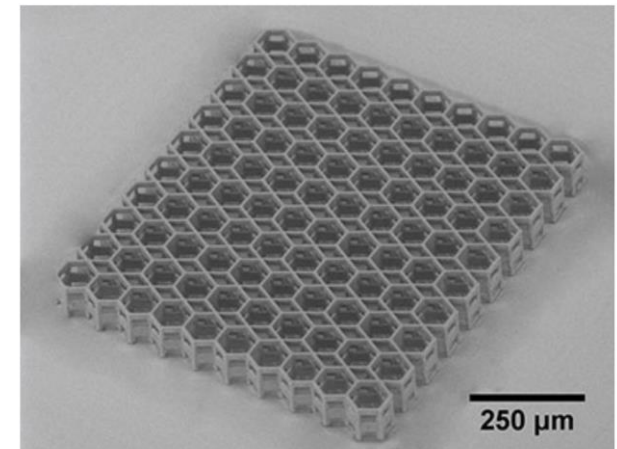


SPECIFICATIONS

Technology	Subtractive manufacturing
Materials	Fused silica, Borosilicate glass
Smallest feature size	$> 1 \mu\text{m}$
Minimum surface roughness	$< 200 \text{ nm}$
Maximum object height	1 cm
Aspect ratio	$> 1:200$
Minimum micro hole diameter	$5 \mu\text{m}$
Writing speed	50 mm/s



Micro Needles



Hexagon Scaffold

Typical materials:

SiO_2

Poly Si

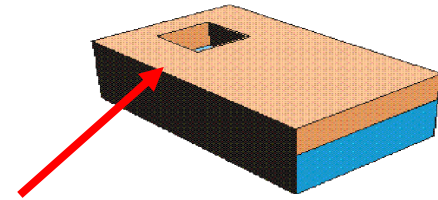
Si_3N_4

Metals

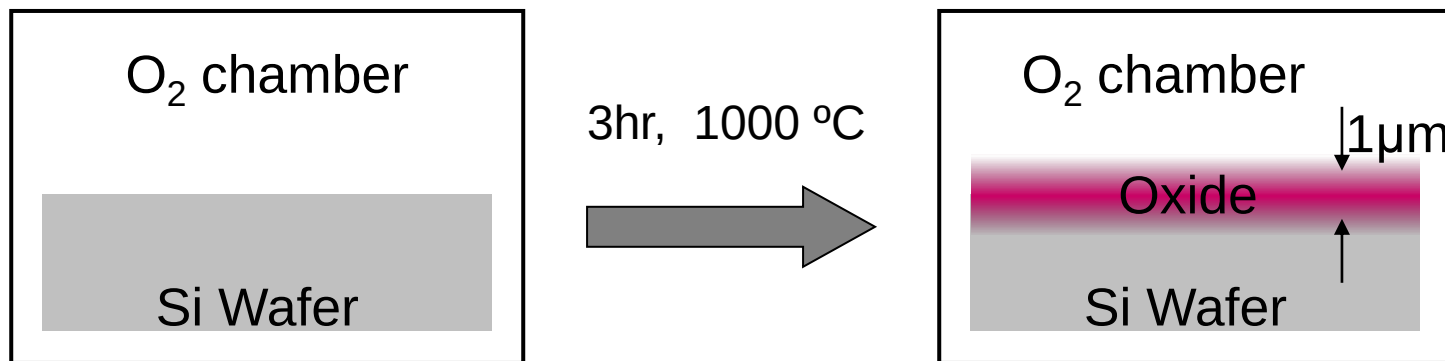
THIN LAYER DEPOSITION

Thermal oxidation (dry)

Forming Silicon Dioxide by oxidation



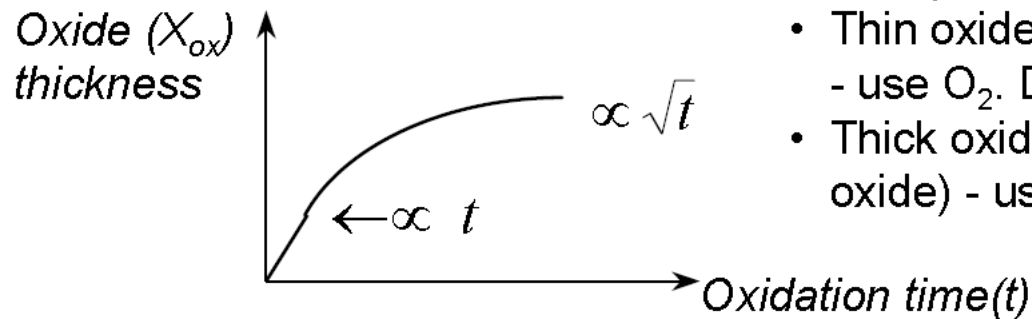
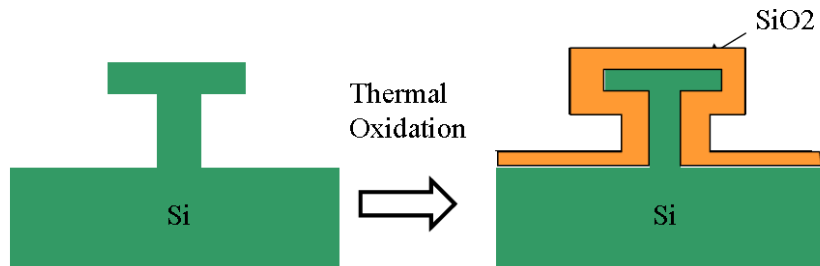
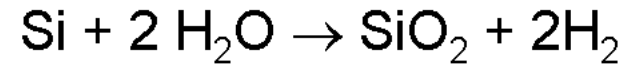
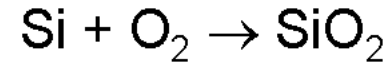
- O_2 chamber @ 800-1200 °C
- Silicon reacts with O_2 to grow oxide



Thermal oxidation: dry vs. wet

- (1) Excellent Electrical Insulator
Resistivity $> 1\text{E}20$ ohm-cm
Energy Gap ~ 9 eV
- (2) High Breakdown Electric Field
 $> 10\text{MV/cm}$
- (3) Stable and Reproducible Si/SiO₂ Interface
- (4) Conformal oxide growth on exposed Si surface

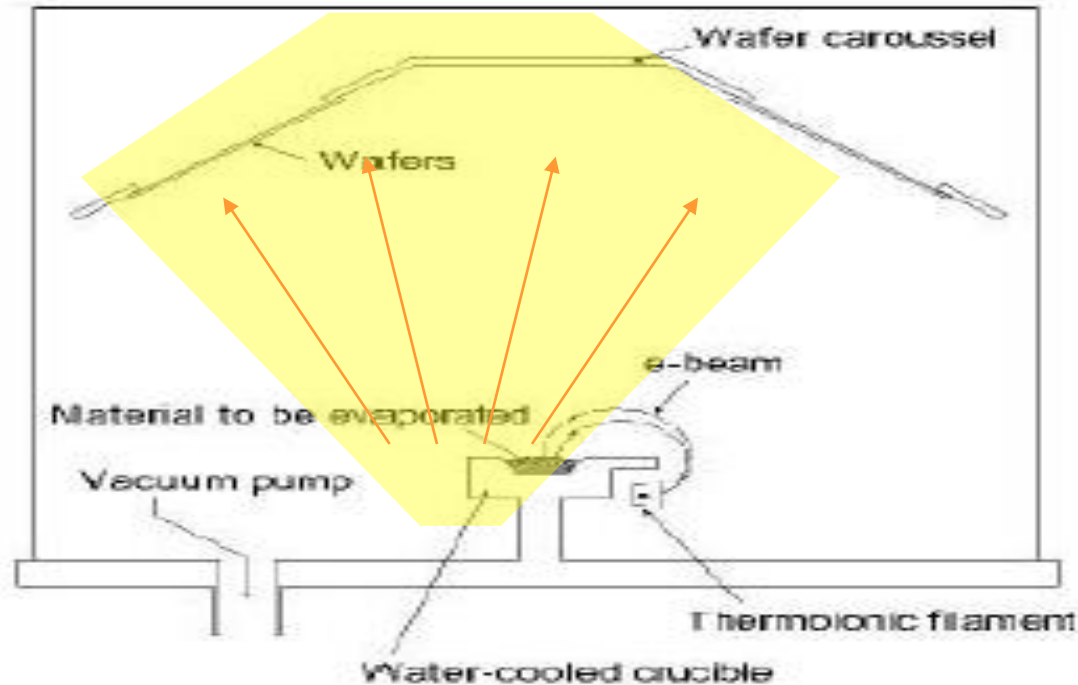
Processing Temperature
900-1100 °C



- O₂ (or H₂O) diffuses through SiO₂ and reacts with Si at the interface to form more SiO₂.
- 1 μm of SiO₂ formed consumes 0.44 μm of Si substrate.
- Thin oxide growth (e.g. gate oxide)
- use O₂. Dry oxidation
- Thick oxide growth (e.g. field oxide)
- use H₂O. Wet oxidation

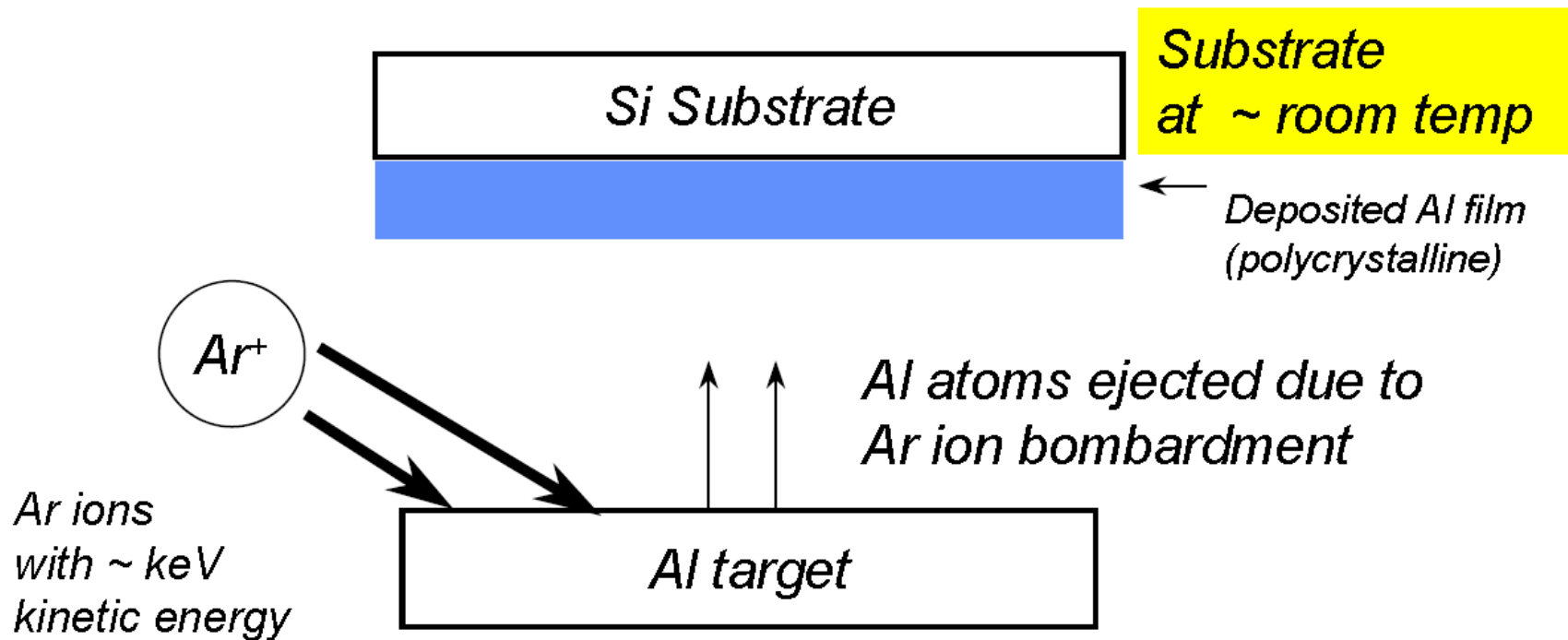
Evaporation

- Metal evaporated w/ electron beam
- Vacuum environment – prevent oxidation, directional vapor travel



Physical vapor deposition

Sputtering Deposition



Physical sputtering

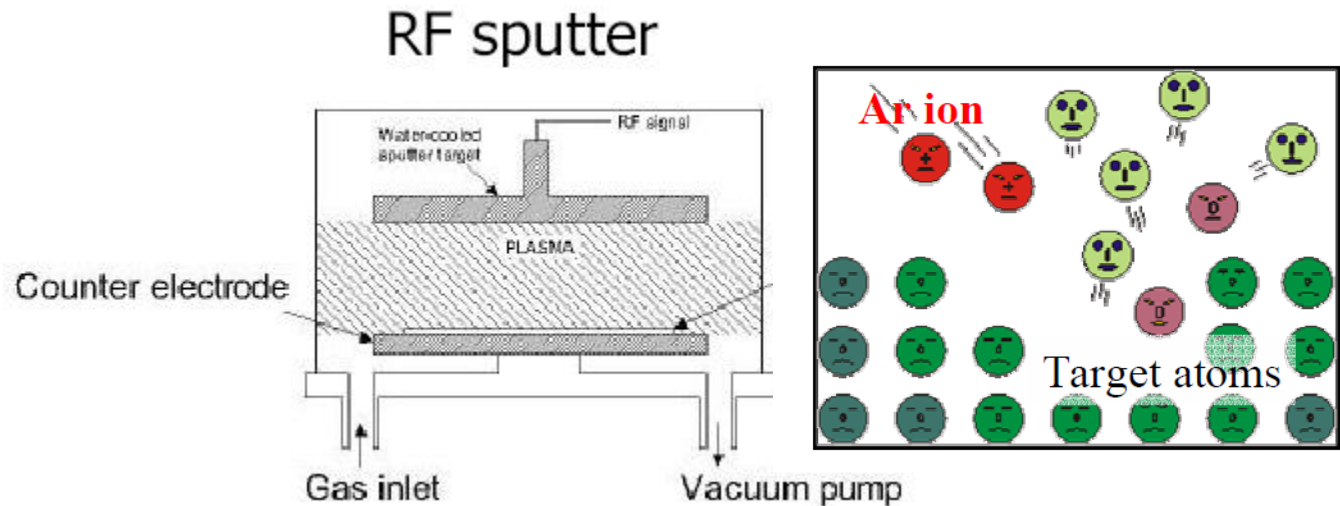
Bombarding the surface with inert ions
(e.g. Ar)

$$1\text{eV} = 1.602 \times 10^{-19} \text{ J}$$

- **$E < 3\text{eV}$** : particles reflected or adsorbed
- **$4\text{ eV} < E < 10\text{eV}$** : some surface sputtering
- **$E > 10\text{-}5000\text{ eV}$** : bond breaking (low P, long mean free path necessary prevent material from redeposition)
- **$E > 10,000\text{ eV}$** : implantation (doping)

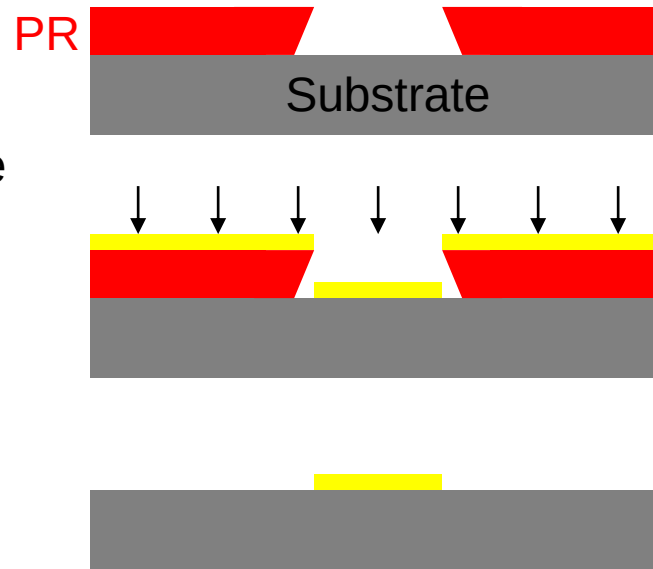
Sputtering

- Materials: Metals and dielectrics
- Requires high vacuum
- Argon ions bombard material target



Reverse resist and lift-off

1. Apply and pattern reverse resist
 - Need negative sidewalls
 - Positive resist – negative image
2. Deposit desired film
 - Evaporation
 - Typically metal
3. Dissolve photoresist, lift-off film

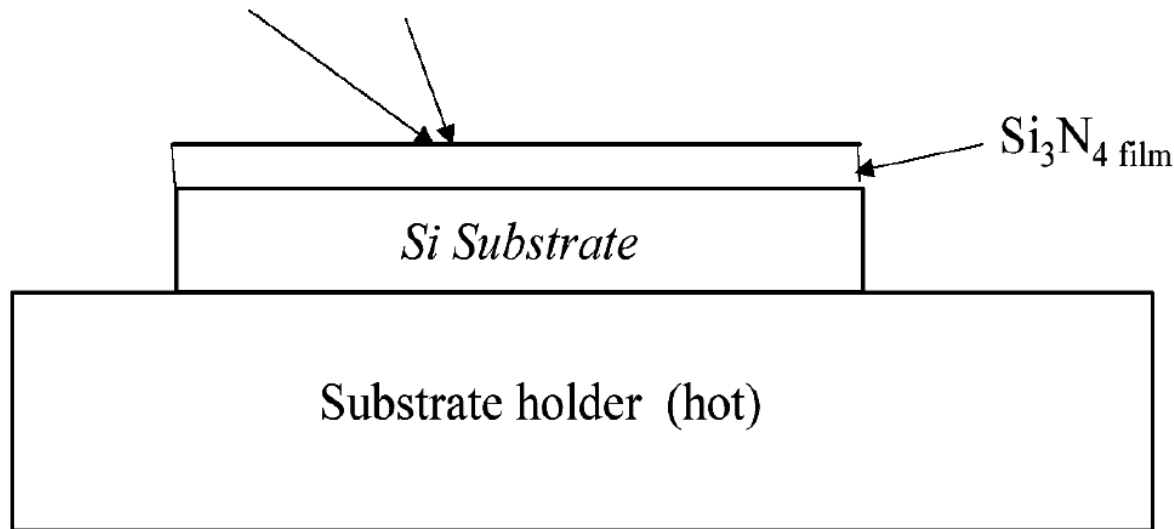
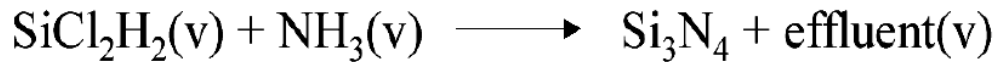


- Limited thickness – need non-conformal film
- Limited deposition methods – PR compatibility
- Not typically used in semiconductor industry

Chemical vapor deposition

CVD, eg. of Si_3N_4

Processing Temperature
300-600°C



Solid films are formed by chemical reactions taking place at the surface.

PE (plasma enhanced) CVD

Ionized chemical species allow a lower T to be used

DIELECTRIC DEPOSITION PROCESSES

	Deposition Temperature	
	LPCVD	PECVD
$\text{SiH}_4 + \text{NH}_3 \Rightarrow \text{Si}_3\text{N}_4$	850° C	200-400°C
$\text{SiH}_4 + \text{N}_2\text{O} \Rightarrow \text{SiO}_2$	800°C	200-400°C
$\text{TEOS} + \text{O}_2 \Rightarrow \text{SiO}_2$	720°C	350°C
$\text{SiH}_4 + \text{O}_2 \Rightarrow \text{SiO}_2$	400°C	

Deposition on 1 side of wafer

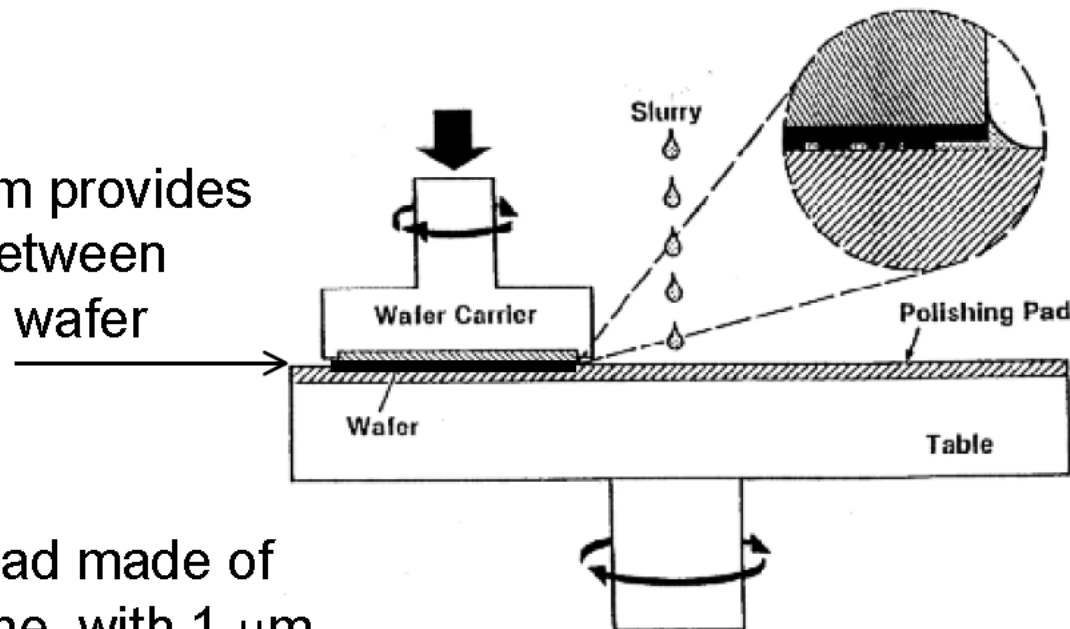
BONDING

Chemical mechanical polishing

Wafer is polished using a slurry containing

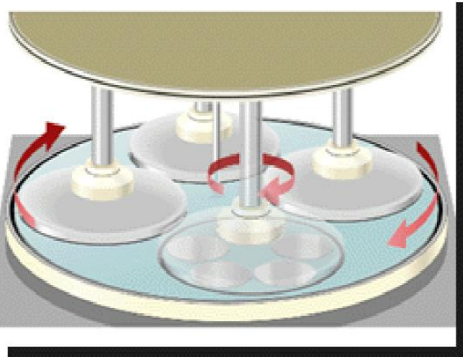
- silica abrasives (10-90 nm particle size)
- etching agents (e.g. dilute HF)

- Backing film provides elasticity between carrier and wafer

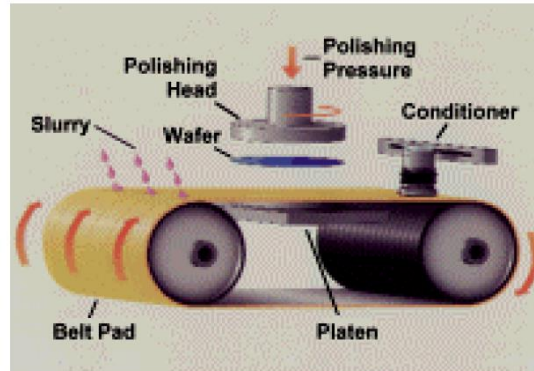


- Polishing pad made of polyurethane, with 1 μm perforations
 - rough surface to hold slurry

CMP



Rotating wafer
Rotating pad



Rotating Wafer
Linear track pad

CMP of	Selectivity to Si_3N_4
SiO_2	6:1
poly-Si	280:1
W	75:1
Al	40:1

Preston Model:

$$\text{Local Removal rate } R = K_p P v$$

where P = local applied pressure

v = relative pad-wafer velocity

K_p = Preston coefficient [unit in pressure^{-1}]

function of film hardness, Young's modulus,
slurry, pad composition and structure

Wafer bonding

Combine complex shapes from multiple wafers

- **Si-Si wafers (direct)**

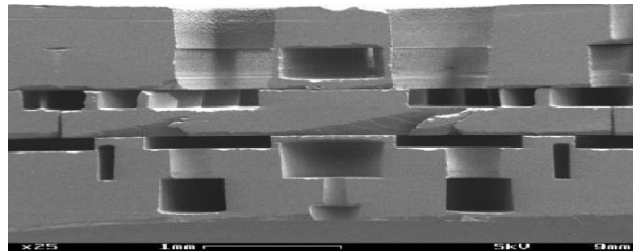
- Low temp (450°C)
- Fusion – high temp (1000°C)

Very flat surface necessary (roughness <0.7nm)

- Adhesive – epoxy, PR

- **Si-Glass wafers**

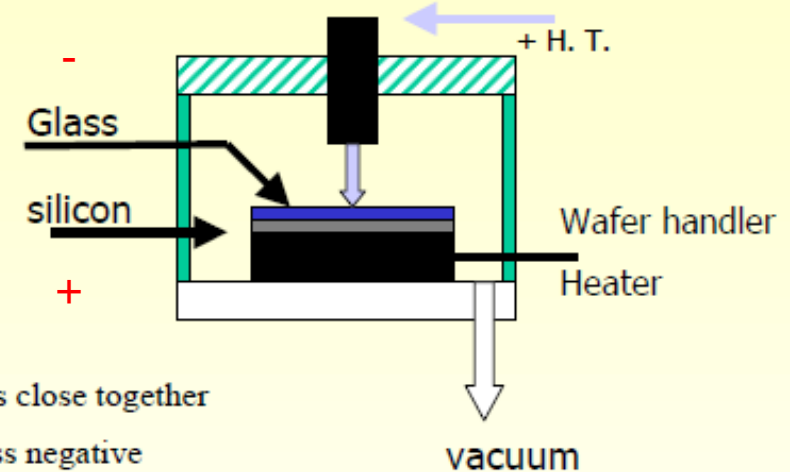
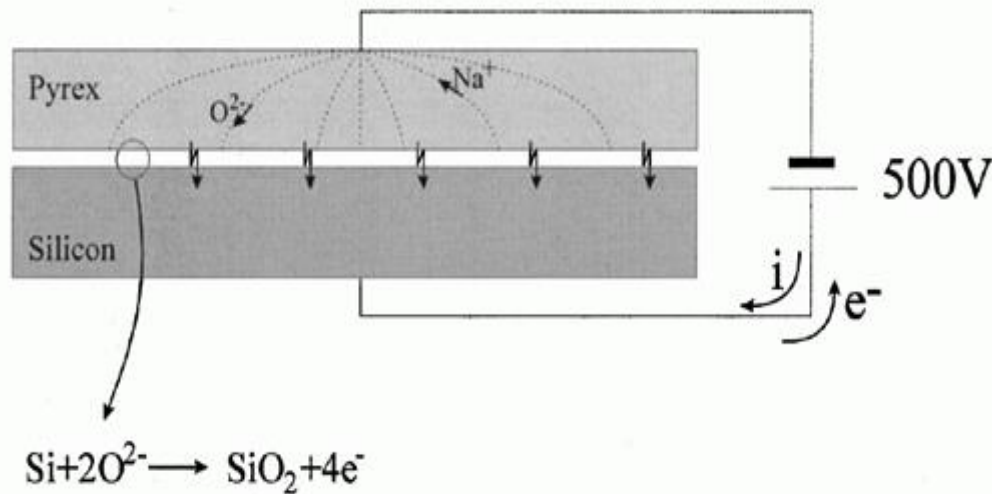
- Anodic – low temp (400°C), high voltage (700V)



Fusion bonded wafer stack



Anodic bonding Borofloat-Si



- Pull silicon and glass close together
- Silicon positive, glass negative
- Use glass with similar thermal expansion coefficient
- Cleanliness critical to prevent voids
- Thin metal lines can pass through bond

Advantages :

- Easy alignment (Glass)
- Low temperature (Can use Aluminum, no impurity diffusion in silicon)

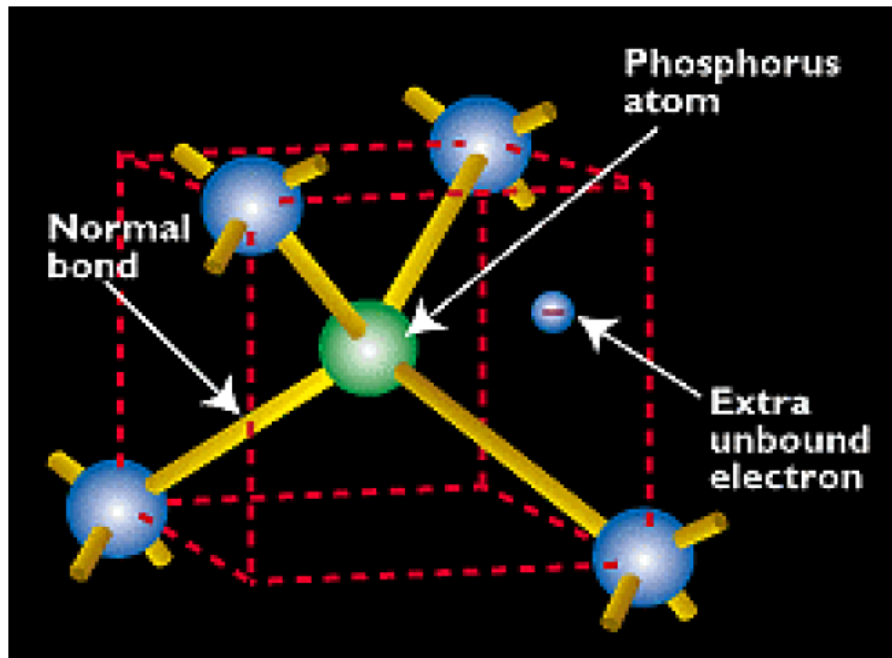
400-700 V
350-450 °C

POROUS MATERIALS

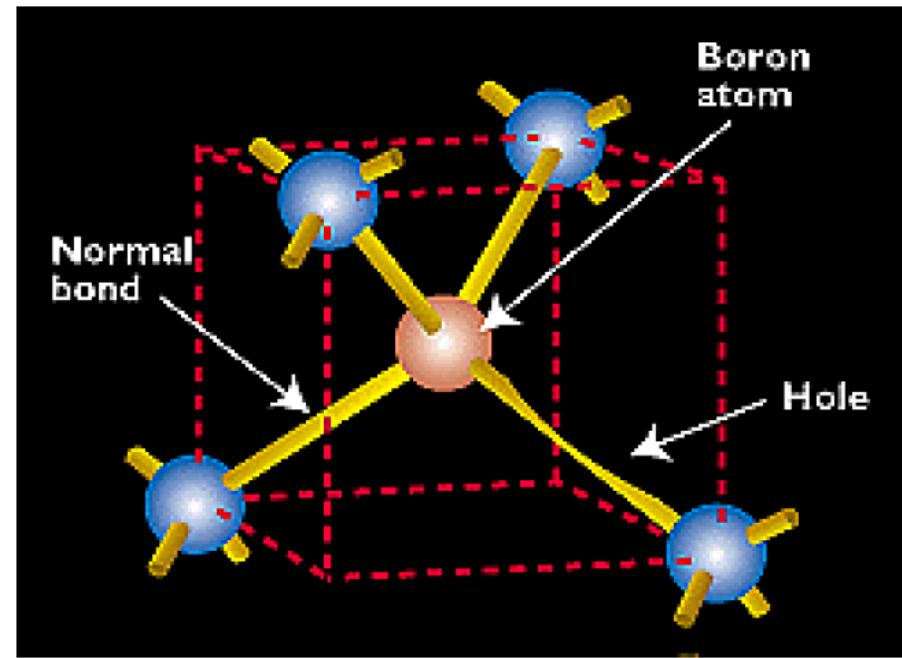
Doping Si

By substituting a Si atom with a special impurity atom (**Column V** or **Column III** element), a conduction electron or hole is created.

Donors: P, As, Sb

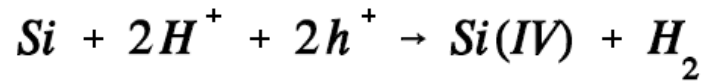
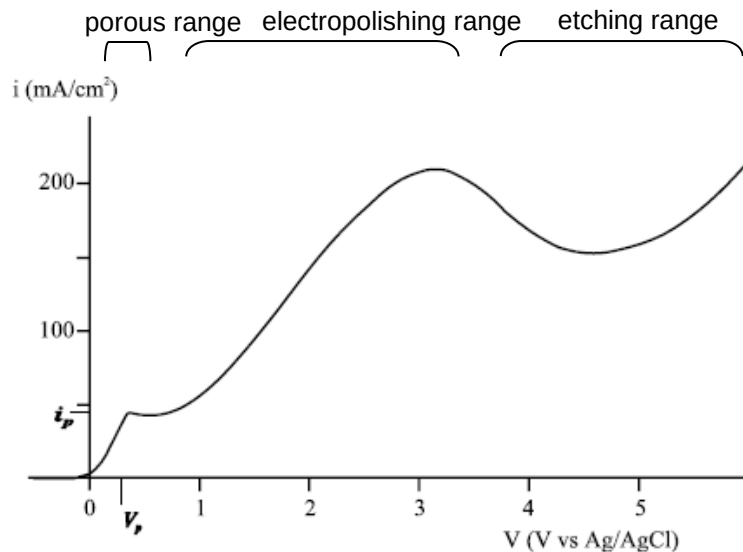


Acceptors: B, Al, Ga, In

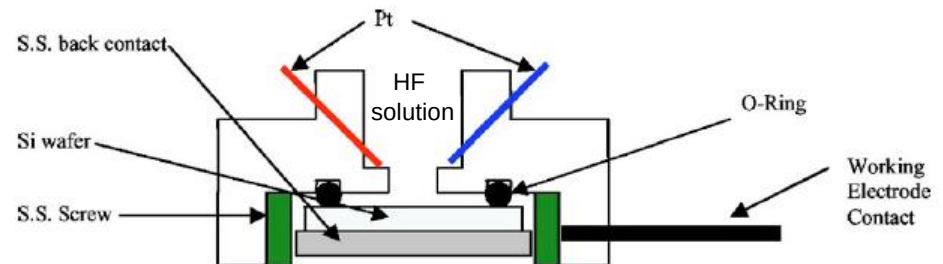


Porous silicon: anodization

Different regimes dependent on current-density



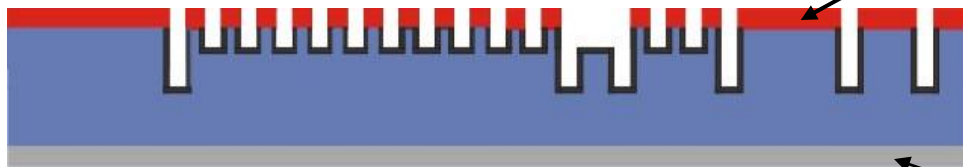
Conditions:
P-type Si



Top protected by SiN to avoid roughening there (bonding issue)

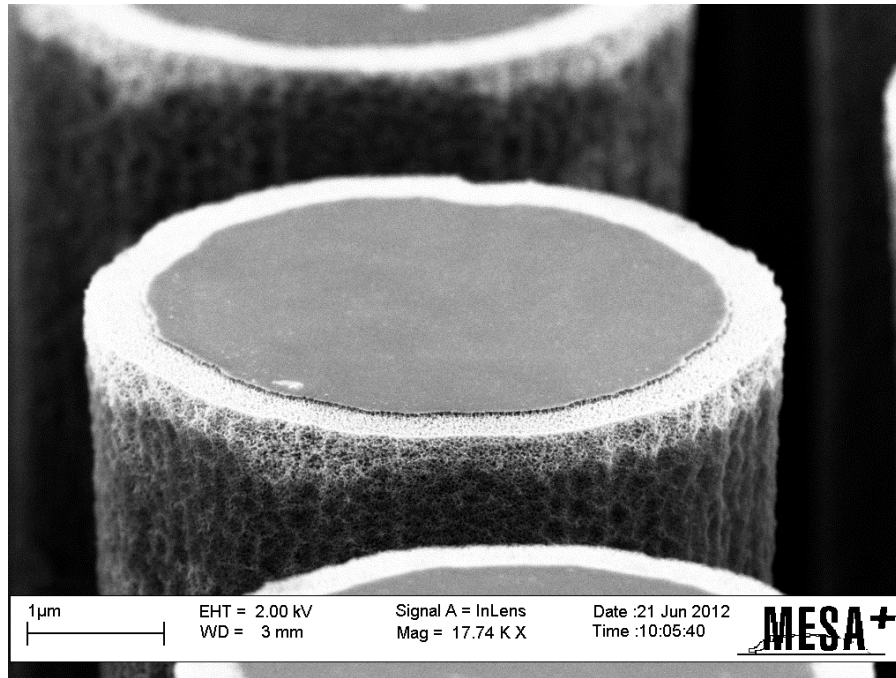
Purging with N₂ during anodization to remove H₂ bubbles

Backside Al: uniform electrical contact



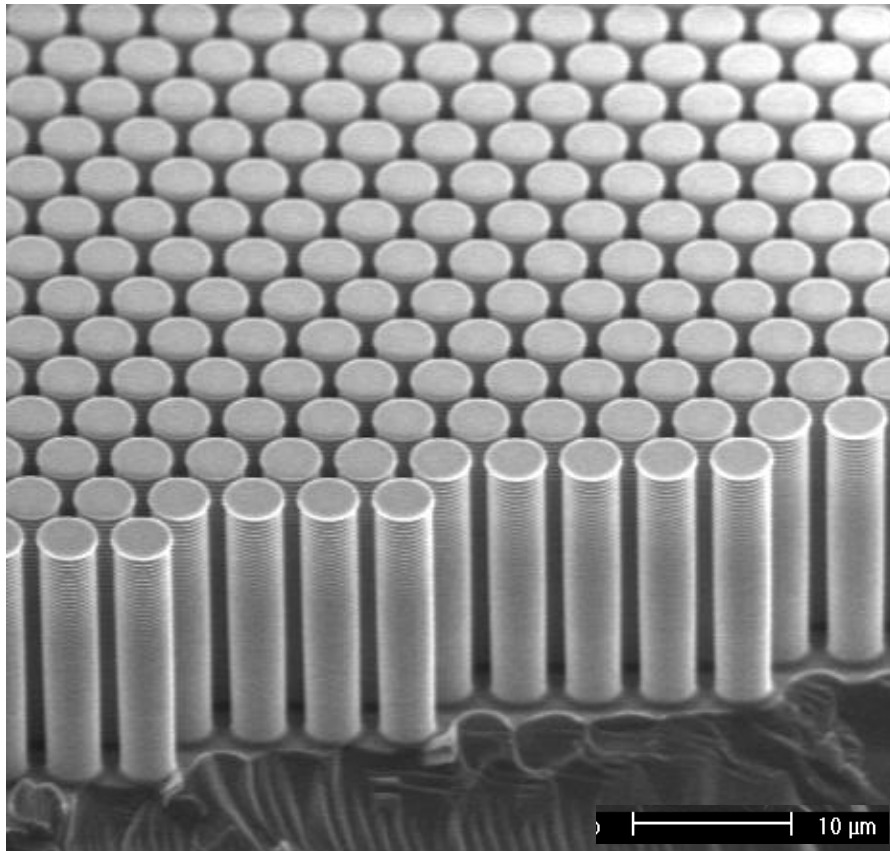
Advantages anodization

- Does not change pillar dimensions (sidewall!)
- Inherently suitable for virtually any column length
- Tunable pores (1- 50 nm)

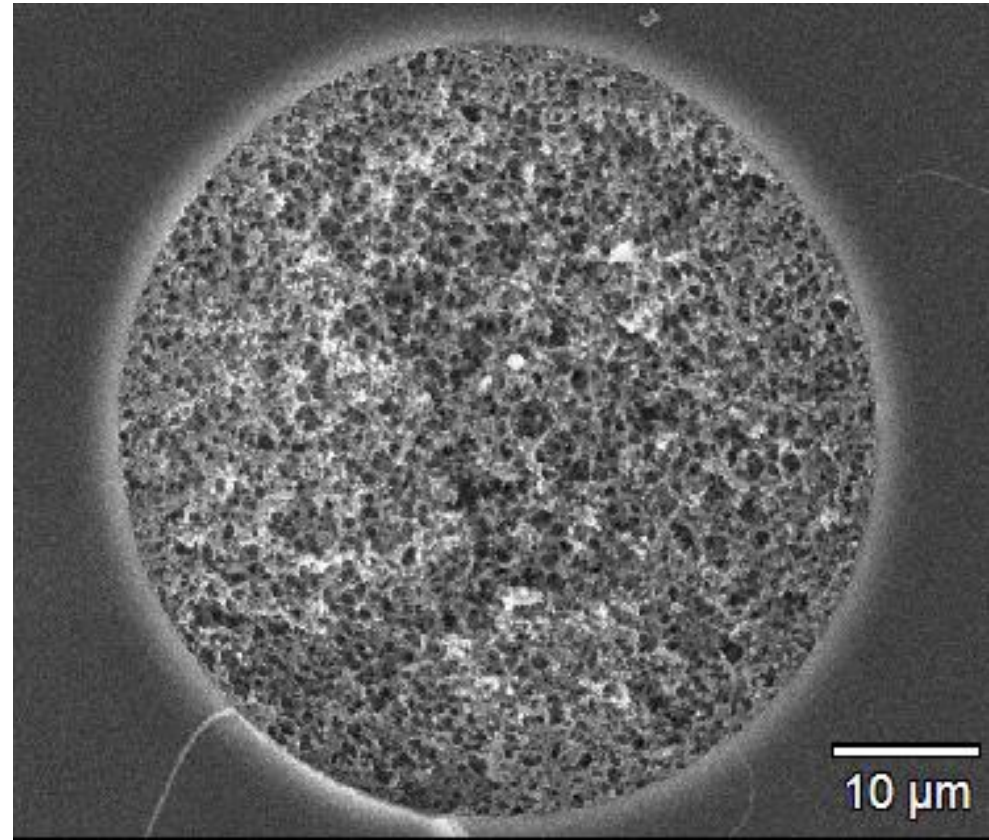


Merging two technologies

2D micropillar array

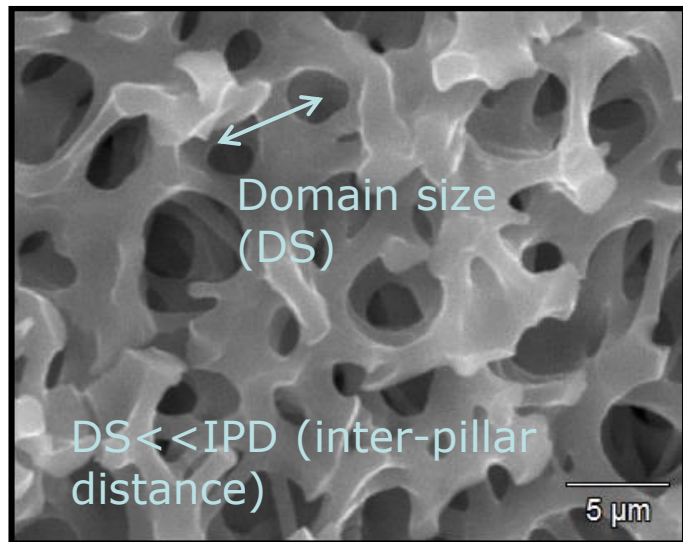
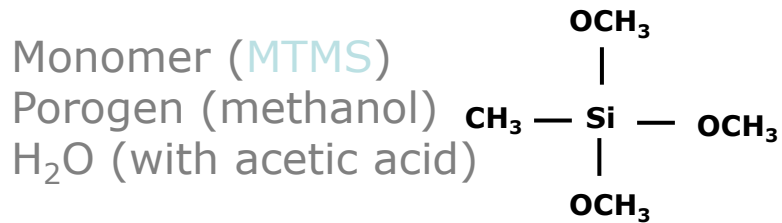


(Silica) Monolith

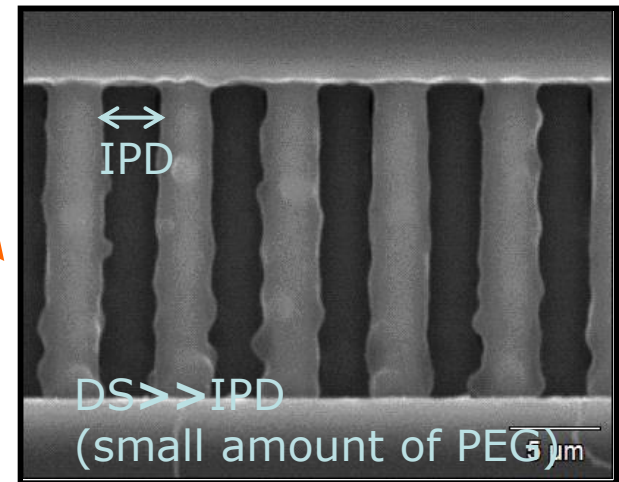
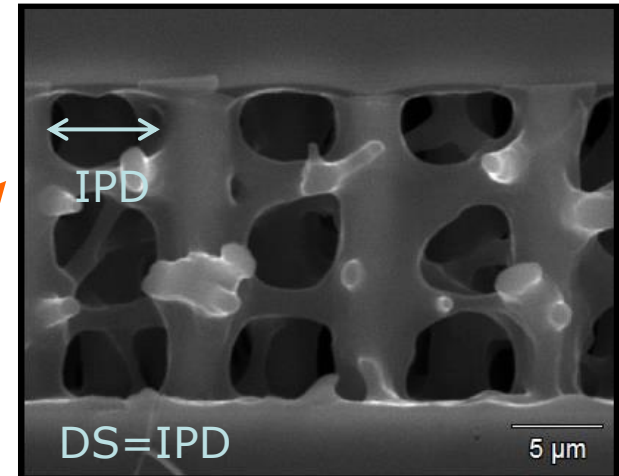


Sol-gel pillars

MTMS: methyltrimethoxysilane



Detobel et al., *J. Chrom. A*, 2009, 44, 7360



Conclusions

- Wide range of μ fabrication techniques available
- Choice depends on:
 - intended separation and detection method
 - compatibility chemicals
- Feature size and shape by lithography and fabrication method
- Incorporation of porous materials is challenging